Research in Reconfigurable Computing: An Industrial Perspective

Juanjo Noguera
Xilinx Research Labs

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Agenda

Why Programmable Logic?

Quick Update on Xilinx Technology

Impact of Research in Industry
Introduction to Xilinx

- **Worldwide Leader in Programmable Logic**
  - Founded in 1984
  - Inventor of the FPGA
  - Pioneer of the fabless model
  - $1.8B in revenues in FY ’09
  - ~3,100 employees worldwide
  - 20,000+ customers worldwide

- **Industry’s first 65 nm FPGAs**
  - Shipping 98% of high-end 65nm production FPGAs in the world

- **Next-generation 40/45nm FPGAs**
  - Virtex-6 & Spartan-6 families
Xilinx Revenue Breakdown

Q2 Calendar Year 2009

Revenue by Geography

- Japan: 8%
- Asia Pacific: 37%
- Europe: 20%
- North America: 35%

Revenue by End Market

- Data Processing: 49%
- Consumer & Auto: 14%
- Industrial & Other: 31%
- Communications: 6%
The Time for Programmable Logic is Now!

Market Forces

- Rapid changing standards
- Time to Market (TTM)
- Fickle, fragmented markets

Programmable Imperative!

- Do more with less
- Reduce risk profile
- Focus on core competencies

Financial Constraints

Technology Innovation

Cost

Power

Performance
"More likely, we will see a large percentage of these questionable designs not hit any production and die a slow death by indefinite push-outs"

_Bryan Lewis, Gartner Analyst_
High Development Costs Driving ASSPs to Ultra High Volume Markets

Development Costs ($M)

Minimum Market Size ($M)

Source: Xilinx, Venture Capital Insights
The Growing ASIC/ASSP Application Gap

- ASIC / ASSP Class Applications
- Traditional FPGA Class Applications
- Underserved Applications

Market Size

Application Market Segments

+ 100s More
Agenda

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Impact of Research in Industry
Modern FPGA Architectures

- Xilinx Virtex-6 and Spartan-6 devices

Efficient Logic
LUT-6 CLB

On-Chip Memory
BlockRAM

High Performance, Low Power
DSP Slices

Abundant resources
Clocking

Virtex-6

550K Logic Cell Device

Spartan-6

150K Logic Cell Device

Enhanced Parallel Connectivity
Parallel I/O

Increased Serial Bandwidth
Transceivers

Built-In
PCIe® Interface

Combination of Flexibility (CLB’s), Integration and Performance (heterogeneity of hard-IP Blocks)
Modern FPGA Architectures

- Xilinx Virtex-6 and Spartan-6 devices

Virtex-6
- Higher Efficiency FIFO Logic
- Built-In Tri-mode EMAC
- Integrated Reliability System Monitor

Spartan-6
- Low Cost Solution Interfacing DDR3
- Integrated Memory Controllers
- Interface to Legacy Systems
- 3.3 Volt compatible I/O

Key differences between both families
## Power Consumption Benefits
- Lowest power operation of any FPGA solution
- 1.23mW/100Mz at 38% toggle rate

## Performance Benefits
- 600MHz operations for any DSP operation including large filters
- ~1.2 TeraMACC in a single device

## Cost Benefits
- Hardened pre-adder and adder cascade saves significant logic resources
- Logic functions can be mapped into DSP blocks
Partial Reconfiguration on Xilinx FPGAs

- Time-multiplex functionality not required at the same time on the Xilinx FPGA
  - Use a smaller device
  - *Reduces cost and power consumption*

Static Implementation

Reconfigurable Implementation
Virtex-5 Configuration Memory Architecture

Reconfigurable modules can be located in the same column

Fast reconfiguration with 32-bit wide 100 MHz V-4 ICAP

Reconfigurable frames are 20 CLBs high

*** Improvements in configuration memory architecture and design flow have enabled wider use of partial reconfiguration ***
Lower Reconfiguration Latencies

Reconfiguration Latency (ms)

~ Order of magnitude improvement in latency when reconfiguring 25% of a XC2VP100 versus 25% of a XCV4LX100

(Both devices have approximately 100,000 logic elements each)
Reconfigurable Encryption/Decryption PRMs
DES/Triple DES cores connected to the PLB bus

Bus Macro
Dedicated slice logic provides communication between static and reconfig modules.

SystemACE Controller
stores bitstreams from a Compact Flash card.

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PLB Arbiter
Arbitrates activity on the On-chip Peripheral Bus

UART
Provides user interface via PC terminal.

PPC405
Program code controls all peripherals and partial reconfiguration activity.

ICAP
Internal Configuration Access Port. Provides interface to config logic.

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*** Key Concepts and Prototypes Developed by German Academics ***
Agenda

Why Programmable Logic?

Quick Update on Xilinx Technology

Impact of Research in Industry
Wired Communication Routers

Customer Needs

- Performance and bandwidth to support 40/100G
- Reduced power consumption
- Flexibility and scalability allow the same FPGA to be used in multiple sockets

Xilinx Value Proposition

- Rapid development and deployment
- FPGA Power reduction = no change to power infrastructure
- Single FPGA platform using multiple configurations replaces multiple ASICs

FPGAs Provide: Low Power, High Performance, Scalable Solution

*** Relevant Market in German Industry ***
FPGA Power-aware Design

- FPGA power optimization can be addressed at multiple levels
- System (Application) and front-end tools can achieve significant power optimizations
- Describe how FPGAs can achieve competitive power advantage when compared to other programmable platforms
  - DSP processors and Network processors
  - Various application domains (e.g., video and networking)
Benefits of Reduced Power Consumption

- **Reduced electricity consumption**
  - Lower operational expenses for the customer

- **Why is heat a bad thing?**
  - Reliability; Speed; Leakage
  - App-specific constraints (size, noise)

- **Heat management solutions**
  - Advanced chip package
  - Heat sink on top of the chip
  - Active fan
  - Spreader plate/heat pipe
  - Liquid immersion

[Intel Tech Journal]
Based on Network Processing Units (NPUs)
- NPUs offer software programmability with high data rates
- But also on CPUs, ASICs, ASSPs, FPGAs

Typical NPU architectures

Intel IXP2805
- Based on multiple processing engines that operate on packets in parallel
  - 16 multi-threaded micro-engines (Intel)
  - 3 multi-tasking processor cores (AMCC)
  - 200-stage programmable pipeline of processor cores (Xelerated)

AMCC nP3700
- Based on multiple processing engines that operate on packets in parallel
  - 16 multi-threaded micro-engines (Intel)
  - 3 multi-tasking processor cores (AMCC)
  - 200-stage programmable pipeline of processor cores (Xelerated)
### Case Study: DSL Access Multiplexer

<table>
<thead>
<tr>
<th>Device</th>
<th>Rate (Gb/s)</th>
<th>Power</th>
<th>Cost</th>
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<tbody>
<tr>
<td>Virtex-4 LX25 32-bit</td>
<td>6.4</td>
<td>&lt;2W</td>
<td>$</td>
</tr>
<tr>
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<td>LSI APP300</td>
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<td>Intel IXP2350</td>
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<tr>
<td>Intel IXP2800</td>
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<td>25.5W</td>
<td>$$$</td>
</tr>
<tr>
<td>Xelerated X11-S200</td>
<td>40</td>
<td>11W</td>
<td>$$$</td>
</tr>
</tbody>
</table>

- Comparable power consumption and price to low-end NPUs
- Performance in the high-end NPU range
Automotive Infotainment and Driver Assistance

Customer Needs

- Deploy scalable solution that supports multiple models
- Provide high level connectivity and entertainment in the automobile
- Meet challenging performance and power requirements

Xilinx Value Proposition

- Use single FPGA platform to replace multiple similar function ASSPs
- Provide low power, scalable programmable environment
- Flexibility to address changing standards and requirements

FPGAs Provide: “Customizable Standard Product”

*** Strong German Industry Leadership in this Market ***
Adaptive Cruise Control & Collision Avoidance

*** Key Concepts and Prototypes Developed by German Academics ***
Partial reconfiguration can be exploited in the automotive domain

- Mutually exclusive applications
Wireless Base Stations

Customer Needs

- Ability to differentiate = Market Leadership
- Reduced power consumption
- Flexibility to adapt to changing wireless standards

Xilinx Value Proposition

- Flexibility and Reduced power consumption
- Performance required for next generation wireless standards

FPGAs Provide: *Flexible, High Performance DSP*

*** Relevant Market in German Industry ***
Industry looking for base station energy reductions (~10% per annum)

**Femtocell drives power and cost reductions**

**Longer-term trends:**
- Multi-mode radio and cognitive radio (increasing adaptability)
- Collaborative communication (diminished base station role)
- Mobility as central feature of Internet (increasing demands)

**Computation and programmability grow, power budgets shrink**
Market Requirements

WCDMA  WiMAX  TD-LTE
TD-SCDMA  FDD-LTE  CDMA2000

Air Interface Standard

2.1GHz  2.5GHz  2.6GHz
2.5GHz  1900MHz
3.5GHz  700MHz

Transmission Frequency

Reduce CapEx / OpEx

↓ Power Consumption  ↑ Transmission eff

Equipment Manufacturers

Multi-Mode BTS

Multi-mode/SDR as common platform strategy to reduce costs and/or increase flexibility
Partial Reconfiguration for Power Savings: Application to the Wireless Domain

- Adapting coding to wireless channel conditions

*** Key Concepts and Prototypes Developed by German Academics ***
FPGA meets processing needs now and expected in 2013 (~172 Mb/s rate), but…

- Only used for some DSP functions and as a co-processor to a DSP processor because:
  - No high-level programming for FPGA, to facilitate scaleable integrated solutions
- And CPU/NPU gets the network processing
High-level Tools for FPGA Design Space Exploration

- Generation of multiple implementations from a single high-level description

- Domain Specific Tools
  - System Generator (DSP)
  - EDK Platform Studio (Embedded)
    - Customize connectivity
  - AccelDSP
    - Matlab to FPGA path

- Recent improvements in general purpose tools
  - e.g., PICO Express (Synfora)
Design Flow
Focus on algorithm functionality, not FPGA implementation details

System Specification (C)
  - Preprocessing & Analysis
  - High-level Optimization
    - (Memory) Optimized Specification (C)
      - Partitioning
        - Functional/Architecture Model (parallel)
          - SW Tuning
          - SW for FPGA
            - Integration
              - Implementation

High-level (C) algorithmic and memory optimizations
  (off-chip transfers, on chip size, #computations)

Exploit and express parallelism

All blocks programmed in C
Using APIs

Rapid iterations over the Design Flow
The Answer: Targeted Design Platforms

Enabling customers to innovate faster...

Focus on Differentiation

Targeted Reference designs

Customer Design

Market-Specific

Domain-Specific

Base Platform

Communication • Video • AVB
Market specific IP, custom tools, custom boards

Embedded • DSP • Connectivity
Domain IP, Domain tools, FMC daughter cards

Virtex®-6 FPGA • Spartan®-6 FPGA
Base IP, ISE program, base boards

Targeted Design Platforms enable developers and designers to focus on differentiation instead of design infrastructure
Summary

- **The Time for Programmable Logic is Now!**
  - Increasing markets segments served by Xilinx FPGA’s
  - FPGA Benefits: Performance, Flexibility, Power efficiency

- **Several Examples of Industrial Impact of this Research Program**
  - Wireless and wired communications
  - Automotive
  - Medical imaging

- **German academics leadership in Reconfigurable Computing**
  - Strategic partnership for Xilinx Research Labs
    - Multiple extended visits to Xilinx San Jose and Dublin
    - Multiple Collaborations with Xilinx business units
Thank you

Juanjo Noguera
Xilinx Research Labs
juanjo.noguera@xilinx.com
+353 1 461 5556