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design

The Erlangen Slot Machine (ESM): A Flexible Platform for Dynamic Reconfigurable Computing

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Introduction

Xilinx FPGAs, one of the few partially reconfigurable devices offer enough logic to efficiently implement resource demanding applications which arise in video, audio and signal processing as well as in other fields like mechanical control. Partial reconfiguration is useful to increase the flexibility in computation and time-sharing of device space. However, this feature cannot be exploited to fully extent on most available systems.

Many systems on the market offer various interfaces for audio and video capturing and rendering, for communication and so forth. However, each interface is connected to the FPGA using dedicated pins in a fixed location. Modules willing to access a given interface like the VGA must be placed in the area of the chip where the FPGA signals are connected. Therefore, the development process of modules for todays FPGAs is very tedious and the relocation even more difficult and not automated.

For example a module placed at a given location on the device is implicitly assigned all the resources in that area. This includes the pins, the clock managers and other hard macros like multipliers and BlockRAM. Each module using resources outside its placement area must have links going through other modules in order to reach the needed resources. This situation has three negative consequences: *1) Module development: Automatizing the development of modules for partial reconfiguration is difficult. 2) Intermodule communication: Placed modules must be able to communicate with other modules independent of their placement position. 3) I/O pin constraints: Modules accessing I/O pins are not relocatable, because each pin has a fixed physical location.*

The purpose of the **Erlangen Slot Machine** is to overcome the deficiencies of existing FPGA platforms by providing:

1. **Maximal reconfigurability through a flexible architecture allowing unrestricted partial reconfiguration**
2. **Module development support**

ESM Architecture

With the limitation of existing platforms in mind, we developed a new platform concept called **ESM**. The platform consists of a **BabyBoard** featuring a Virtex II 6000 FPGA from Xilinx, several SRAM banks and a configuration circuit. The flexibility of partial reconfiguration is maximized here by providing a separable BabyBoard which can be mounted on different **MotherBoard** types.

ESM BabyBoard

The main components on the BabyBoard are:

1. The main FPGA: Xilinx Virtex II 6000/8000 FPGA connected to different interfaces.
2. Configuration circuit which consists of an FPGA Spartan II used to configure the main FPGA and a CPLD used to download the Spartan II configuration on power up.
3. A Flash with 64 Mbyte capacity is available to enable the storage of up to 32 full configurations.

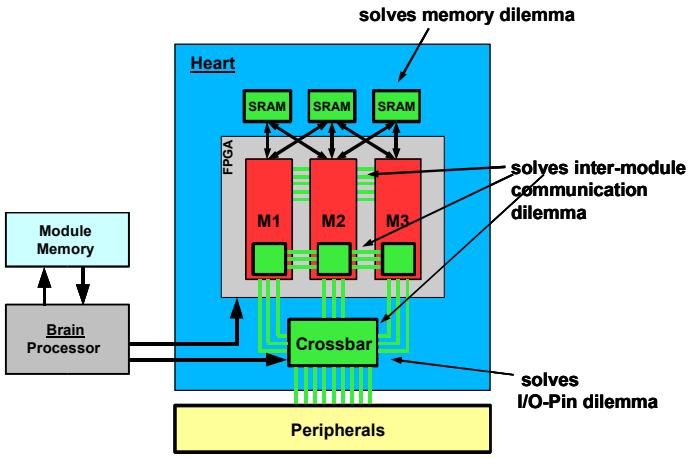

Figure 1: ESM Architecture overview

4. Six SRAM banks with 2 Mbyte each are vertically attached to the board, thus providing enough memory space to six different slots for temporal data storage. The SRAMs can be also used for shared memory communication between neighbor modules, e.g., for streaming applications. The SRAMs are connected to the FPGA in such a way that the reconfiguration of a given module will not affect the access to other modules. The connection to the SRAMs is realized in the north of the device.
5. Interface Access: Interface pins are available in the south of the device. Several modules placed on the device can therefore access their interface devices like video and audio input and output, high speed communication, etc. using the south ports. The connection to the interfaces is dynamically switched through a run-time programmable FPGA on the MotherBoard realizing the interface controller.

ESM MotherBoard

We currently provide only one type of MotherBoard that is mainly targeted to develop applications in multimedia and signal processing. The MotherBoard provides programmable links to all peripherals.

Their links are established through a programmable crossbar implemented in a dedicated FPGA. This crossbar functionality basically solves the I/O pin dilemma of all existing FPGA platforms, thus allowing free relocation of modules requiring I/O pin connectivity. Free module relocation is possible via a configuration manager on the BabyBoard.

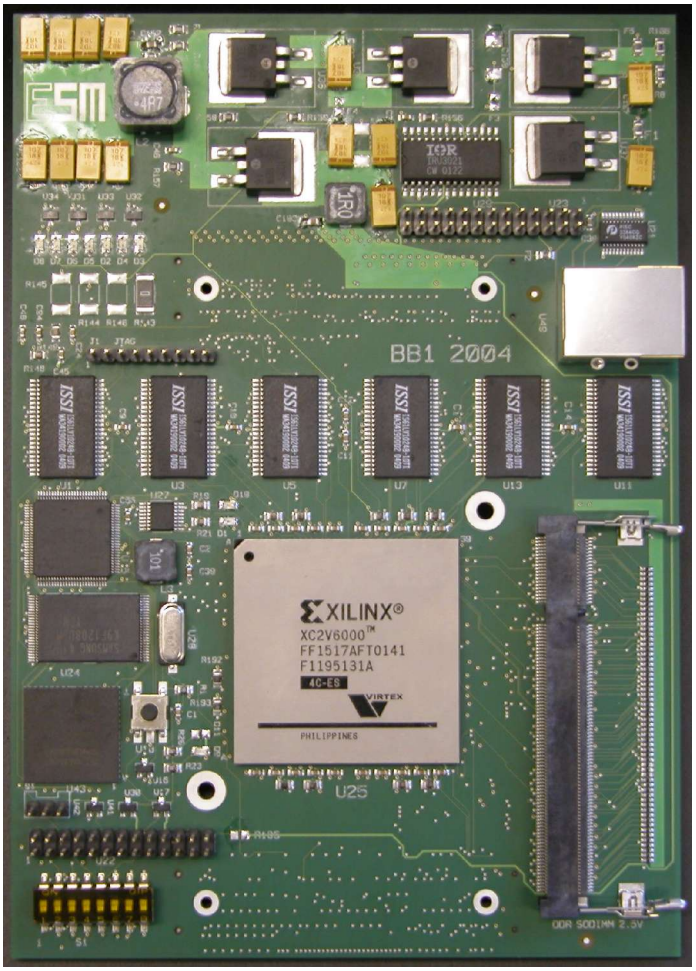

Figure 2: ESM BabyBoard

ESM Middleware and SlotComposer

The ESM is a complete platform containing the two boards FPGA system as well as all middleware APIs and a design automation tool called SlotComposer. After building the application consisting of multiple modules, the tool SlotComposer can be used to generate the required wrappers which are needed for using the four supported communication types illustrated in Figure 1 without writing any code.

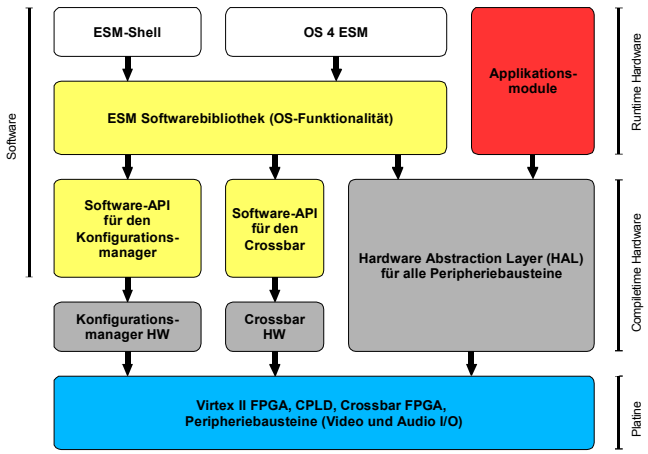

Figure 3: The ESM Platform will provide all middleware APIs thus accelerating the creation of dynamically reconfigurable applications.

ESM Technical Data

Virtex II FPGA	XC2V-6000/8000
Crossbar Link	264 bit at 66 MHz equal to 2.02 GByte/s
Memory SRAM DDR SDRAM Flash	 6 banks of 2 MByte asynchronous SRAM user defined, up to 512 MByte 64 MByte
I/Os Debug General Purpose	 24 bit I/Os and JTAG 117 bit
Freely groupable basic slots	22 of 2 CLBs (8 slices) each
Configuration	JTAG, Flash, EPP

Figure 4: ESM6000 BabyBoard specification

Embedded PowerPC	MPC875 running at 133 MHz
Crossbar Link	264 bit at 66 MHz equal to 2.02 Gbyte/s
Crossbar FPGA	XC2S600E
Memory PowerPC SDRAM PowerPC Flash Video RAM FPGA Flash	 64 MByte 16 MByte 4 MByte 2 MByte
I/Os Debug General Purpose from BabyBoard IEEE1394 Audio Video Ethernet USB	 BDM and JTAG 117 bit 2 FireWire interfaces Analog stereo In/Out TV Video Encoder/Decoder, RGB and DVI Out 100 Mbit port USB 1.0 port on the go
Configuration	JTAG, Flash, BDM

Figure 5: ESM6000 MotherBoard specification

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