10G Ethernet Controller for Accelerated Stream Processing

With the advent of IoT and Industry 4.0, not only is the amount of data increasing, but also the real-time requirements for its processing. The ReProVide project targets to overcome these new challenges with the help of FPGAs. These can be used in data centers as intelligent switches and smart NICs (Network Interface Cards) to deploy accelerators for downstream operations directly in the data stream.

To enable such a deployment, it is necessary to process the incoming network packets directly on the FPGA. For this purpose, a UDP/IP stack is to be set up in hardware. Based on the UDP protocol, a lightweight protocol for communication with the FPGA shall be developed to support essential functions of the TCP protocol (detection of losses, order of packets, etc.), however without covering the full complexity of TCP.

Prerequisites: Basic knowledge in C++, Python, VHDL and ideally Verilog
Type of Work: Theory (20%), Conception (30%), Implementation (50%)
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