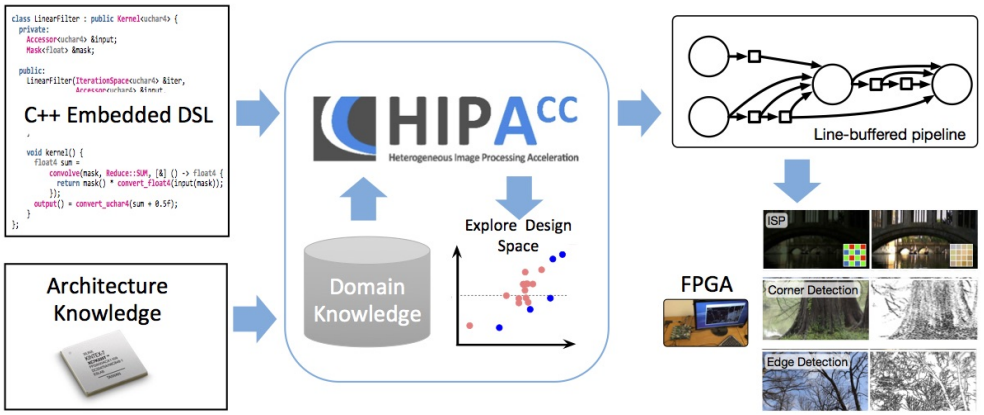
DSL-Based Optimization of FPGA Implementations

FPGAs have proven to be among the most suitable devices for algorithms that can be processed in a streaming pipeline. Yet, designing imaging systems for FPGAs remains a time-consuming task even for an expert. Furthermore, a designer faces various choices while accelerating a particular algorithm, all of which lead to different implementations in terms of performance, area, and power. This hinders portability of the hardware design across different FPGA devices, which have different constraints e.g. area, on-chip memory, and speed.



How to optimize an implementation under certain design objectives and keep portability? A solution could be to use a domain-specific language (DSL), e.g. HIPAcc, to describe an algorithm and let a compiler generate optimized solutions for the specified device and certain constraints. The aims of thesis are: a) building up a tool set for image processing applications to apply state-of-the-art design techniques for FPGAs using Vivado HLS, such as strength reduction, kernel fusion, data-path compression. b) integrating the developed tool set into HIPAcc, and c) developing a design space exploration mechanism.

Required skills:	Good knowledge of C/C++, and basic knowledge of FPGA development
Nature of work:	Theory (30 %), Conception (30 %), Implementation (40 %)
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