Implementation and Analysis of a Sequential Approximate Multiplier

During the design of embedded systems, many design decisions have to be made to trade off between the conflicting objectives of minimizing power consumption and maximizing performance. Approximate computing allows to optimize both objectives, for the sake of accuracy. This means that an error in computation may be tolerated as long as it is small enough to maintain a feasible operation of the system.

In this thesis, the principle of approximate computing shall be applied to the design of a high-performance approximate multiplier unit implemented in an FPGA. The trade off between accuracy and performance will be investigated, varying the amount of accurately and approximately evaluated bits. Different experiments to compare gains and overheads are going to be conducted. Thus, conventional arithmetic structures will be modified to perform approximate operations, aiming to achieve said comparisons.

Prerequisites: Programming skills in VHDL (C and Matlab preferred but not essential)
Type of Work: Theory (50%), Implementation (50%)
Supervisor: Jorge Echavarria (jorge.a.echavarria@fau.de)