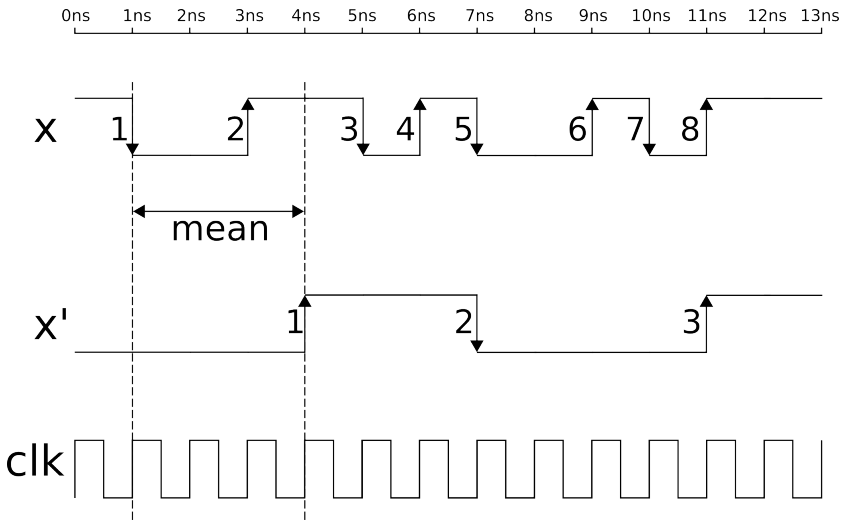
Intelligent Net Gating for Power Consumption Optimization in Approximate Architectures

Clock gating is a very well known power optimization technique employed in both ASIC and FPGA designs to reduce unnecessary switching activity. Approximate computing allows us to take one step forward. By identifying the signals in a set of possible candidates to be approximated with a higher probability of switching activity and high fanout, we can reduce their contribution to power dissipation by net gating.



In this thesis, the principle of approximate computing shall be applied to the design of switching averaging instrumentations. Different experiments to compare gains and overheads are going to be conducted. The trade off between accuracy and power consumption will be investigated, presenting a wide range of evaluations.

Prerequisites:	Programming skills in C++ and VHDL (Matlab preferred but not essential)
Type of Work:	Theory (30%), Conception (20%), Implementation (50%)
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