

# Flexibility/Reconfigurability Trade-offs in SDR Architectures

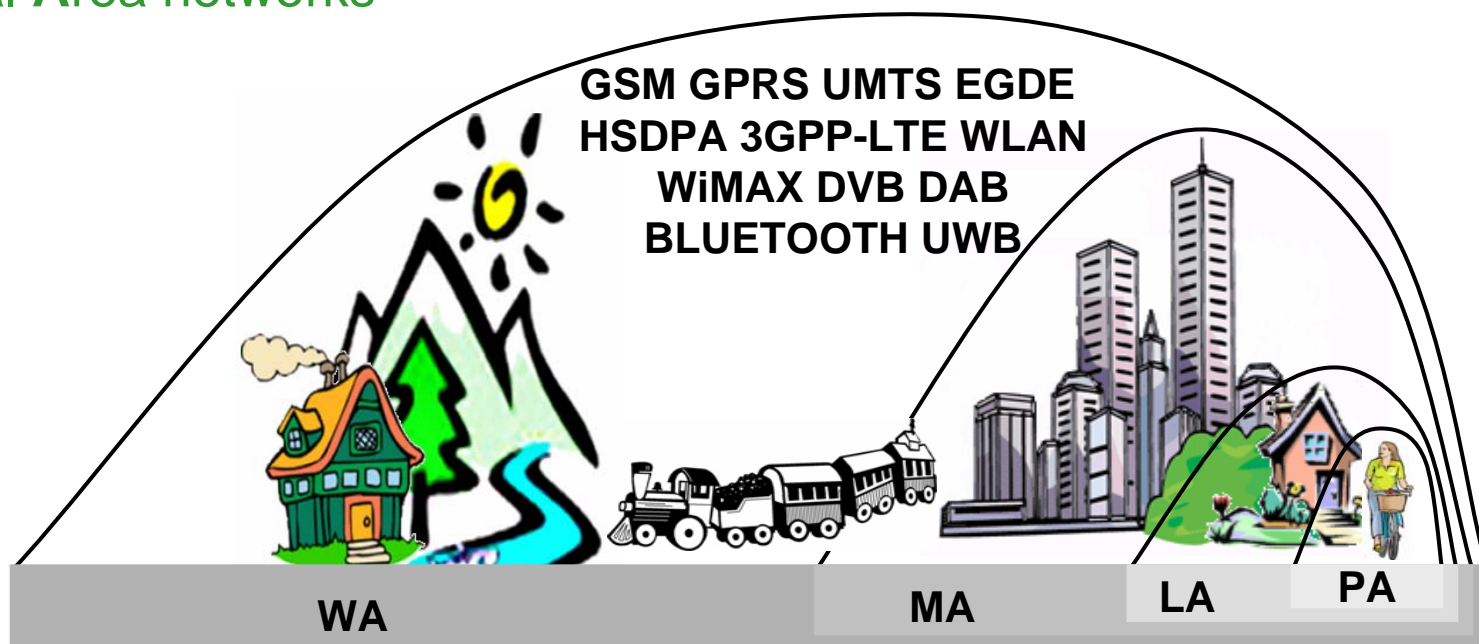
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# Entwurf einer dynamisch rekonfigurierbaren Plattform für Kanalcodierung zukünftiger Mobilfunksysteme

Wide Area networks  
Metropolitan Area networks  
Local Area networks  
Personal Area networks

Consumer application  
Time-to-Market  
NRE-costs Silicon-costs  
Low-Power Volume



Connection any where, any time, any one, any information

# Project Overview

## Phase 1 (2005-2007)

- Implementation of dynamically reconfigurable decoder for trellis based decoding algorithms - FlexiTreP
- First studies on High-Throughput

## Phase 2 (2007-2009)

- Optimization of FlexiTreP architecture
- Silicon Implementation of FlexiTreP (65nm technology)
- Enhancement of platform for flexible LDPC decoding
- High-Throughput
- Consideration of Reliability Issues in the platform design

# Software Defined Radio (SDR)

## Flexibility requirements

- Multi-Standard
- Multi-mode e.g. uplink UMTS, downlink DVB-H
- Evolution of standards e.g. UMTS/HSDPA
- Upgrading in the field
- Adaptivity - „Cognitive Radio“

## Software Defined Radio

- Flexibility of baseband processing in air interface by software

## Flexibility/Cost trade-off

- Especially energy gap
- Standard processors infeasible
  - 20 GOP @ 1400mAh -> GPP @ 40 sec active
- *Flexibility only when valuable!*

# Inner Modem Flexibility

## Filters

- Techniques in standards similar
- Standard signal processing, regular and simple algorithms
- **Software flexibility yields no benefit**

## (De)modulation & Channel Estimation

- Techniques in standards different
- Standard signal processing but complex algorithms
- **Software flexibility brings benefit**

## Programmable (reconfigurable) SIMD/Vector engines

- Sandblaster (Sandbridge), MUSIC Architecture (Infineon)
- EVP (NXP), SAMIRA (Univ. Dresden), SODA (ARM, Univ. Michigan)...
- SDR ADRES architecture (IMEC)
- MONTIUM (Univ. of Twente)

# Outer Modem Flexibility

## Encoding/Decoding

- Techniques in standards
  - Convolutional Codes, Turbo-Codes, LDPC Codes
- Complex (iterative) decoding algorithms
  - Non standard signal processing
  - Non standard arithmetic
  - Non-standard wordwidth
- Efficient data management is challenging
  - Bandwith, transfer, storage
- Flexibility required
  - but limited value of high-level software flexibility

# Standards/Flexibility

Standard	Codes	Rates	States	Blocksizes	Throughput*
<b>GSM</b>	CC	3/4...1/4	16, 64	33...876	...12 kbps
<b>EDGE</b>	CC	6/7, 1/3	64	39...870	5...62 kbps
<b>UMTS</b>	CC	1/2, 1/3	256	1-504	...32 kbps
	bTC	1/3	8	40-5114	...2 Mbps
<b>HSDPA</b>	bTC	1/2...3/4	8	40-5114	...14.4 Mbps
<b>LTE</b>	bTC	1/3	8	40-5114	...100Mbps
<b>CDMA-2k</b>	CC	1/2...1/6	256	1-744	...28 kbps
	bTC	1/2...1/5	8	378...20736	...2 Mbps
<b>IEEE802.11 a,b,g,n (WLAN)</b>	CC	1/2...3/4	64	1...4095	6...54 Mbps
	CC	2/3	256		...300 Mbps
	CC	1/2...5/6	64		...450 Mbps
	LDPC	1/2...5/6	-	...1944	...450 Mbps
<b>DAB</b>	CC	1/4	64	1...4095	1.1 Mbps
<b>IEEE802.16 (WiMax)</b>	CC	1/2...7/8	64	...2040	...54 Mbps
	dbTC	1/2...3/4	8	... 648	...54 Mbps
	LDPC	1/2...5/6	-	...2304	~100Mbps
<b>DVB-T/H</b>	CC	1/4 ...7/8	64	1624	...32 Mbps
<b>DVB-RCT</b>	dbTC	1/2, 3/4	16	...648	...31Mbps

\* Throughput/Channel

# Flexibility/Performance Trade-Off

- **Weakly programmable decoding engine based on ASIP**
  - „Just enough flexibility“
  - Start on block architecture level, not on C-Code level
  - „ASIP unlimited“
    - No constraints on instructions, pipeline, memory structure

## **Exploit programmability**

- Instruction level flexibility
- Decoding algorithms e.g. Log-MAP, Viterbi

## **Exploit hardware reconfigurability**

- Efficient data management
- Fast context switching and multi context instructions

# FlexiTreP Features

**Supports all trellis-based decoding techniques in current standards**

Binary *Turbo-Code* Decoding

- Constraint length between 3 and 5
- Arbitrary generator and feedback polynomials
- Rates down to 1/5 (bTC) and 1/3 (dbTC)
- Interleaver table loadable

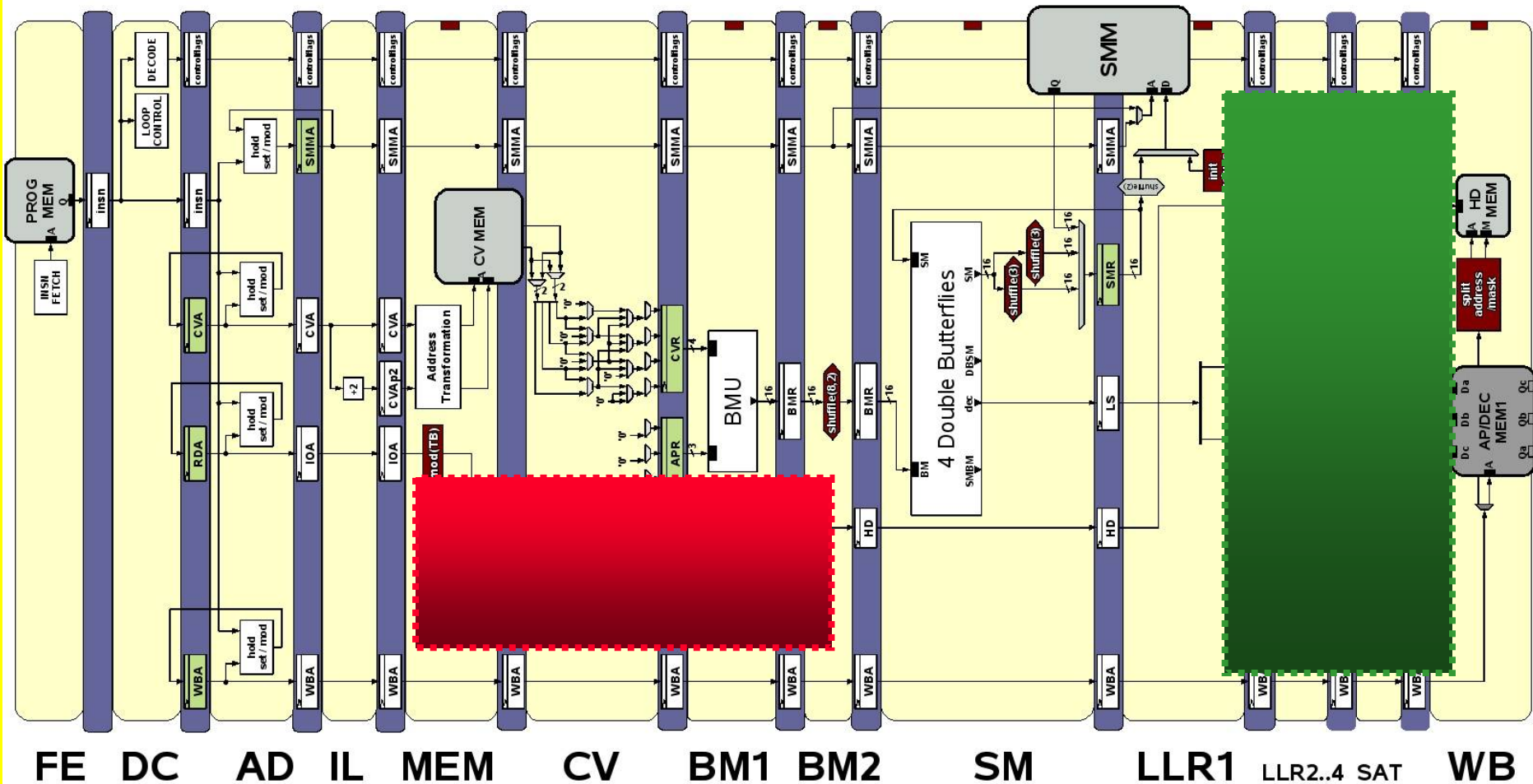
Binary MAP and Viterbi decoding for *Convolutional codes*

- Constraint length between 5 and 9
- Arbitrary generator and feedback polynomials
- Rates down to 1/4



# FlexiTreP configured for Viterbi Decoding

## Dynamically reconfigurable Channel Code Control



# (Re)Configurability

## Two Types of configurability

- Design-time configurability
- Run-time (re)configurability

	Design-time	Run-time
Codeclass (CC, TC..)	X	
Codestructure		X
Algorithm (VA, MAP..)	X	X
Memory	X	X

# Synthesis Results

- Various ASIP instances with different functionality

Functionality	Standard cells (65nm)		FPGA (Xilinx xc4vlx80-12)	
	Area [ $\mu\text{m}^2$ ]	Frequency [MHz]	Slices	Frequency [MHz]
bTC, dbTC, VA (H/S CC)	109320	400	7012	109
bTC, dbTC, VA (H CC)	106762	400	6683	112
bTC, dbTC (dbTC only 8 states)	88966	415	5494	117
bTC	74391	450	4207	135

- Sum of all memories in 65nm: 313000  $\mu\text{m}^2$



**ASIP smaller than 0,5mm<sup>2</sup>**

# Performance Comparison

	Technology	Frequency	Size
STM ST120	130nm	200MHz	~200kGE
Conf. RISC	130nm	133MHz	~100kGE
SODA	180nm	400MHz	~1000kGE
ASIP (ENST)	90nm	335MHz	97kGE
FlexiTreP	65nm	400MHz	53kGE

	UMTS bTC		WLAN VA	DVB-RCS dbTC	
	Cycles/bit @5iter	Throughput @5iter	Throughput	Cycles/bit @5iter	Throughput @5iter
STM ST120	370	0.54Mbps	?	?	?
Conf. RISC	90	1.4Mbps	?	?	?
SODA	200	2Mbps	24Mbps	?	?
ASIP (ENST)	65	5Mbps	---	37.5	8.6Mbps
FlexiTreP	23.5	17Mbps	44Mbps	11.8	34Mbps

# Standards/Flexibility

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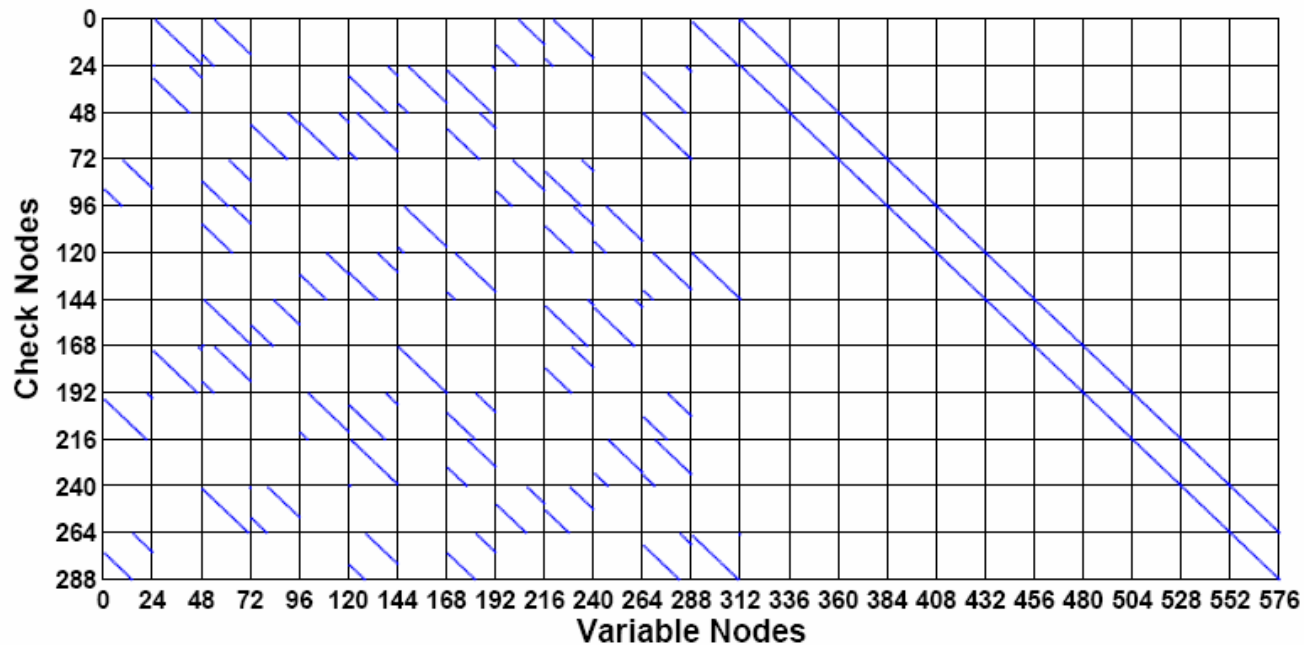
\* Throughput/Channel

# LDPC ASIP

- LDPC decoding strongly differs from trellis based decoding

$$H\vec{x}^T = \vec{0}$$

- Iterative decoding based on „structured“ parity-check matrices



- Submatrix sizes determine parallelism of LDPC decoder

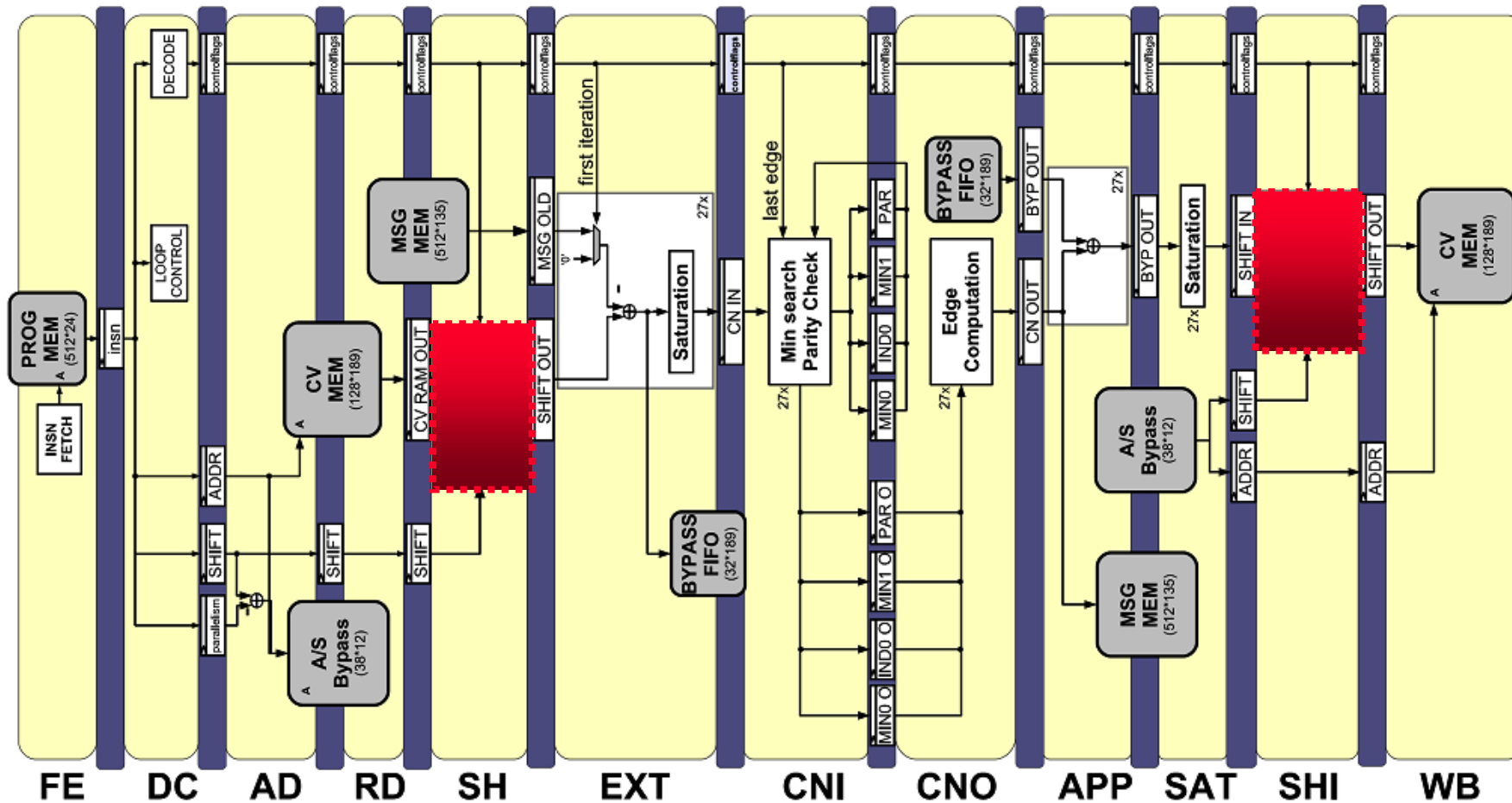
# UKL LDPC Decoder Implementations

LDPC Code	DVB-S2		WiMAX (802.16e) WiFi (802.11n)	U-S LDPC
Codeword Size	64800		576-2304	9600
Code Rate	1/4-9/10		1/2-5/6	3/4
Parallelism	90	360	1-32	80
Quantization	6 bit			
Algorithm	3-Min		MinSum + ESF	
Max. Iterations	50-15		20-10	7
Architecture	1-phase	PN branch	Layered	
Clock frequency	400 MHz		500 MHz	
Area [mm <sup>2</sup> ] 65nm CMOS				
VNP	0.13	0.22	0	0
CNP	0.33	1.20	0.14	0.24
Network	0.05	0.27	0.01	0.03
Memory	3.36	4.43	0.26	0.37
Overall Area	3.87	6.12	0.43	0.66
Net Throughput	60-708 Mbps	0.23-2.68 Gbps	66-376 Mbps	1.54 Gbps
Latency	270-82 $\mu$ s	69-21 $\mu$ s	4.4-5.1 $\mu$ s	4.7 $\mu$ s
Max. Efficiency	183 Mbps / mm <sup>2</sup>	430 Mbps / mm <sup>2</sup>	874 Mbps / mm <sup>2</sup>	2.3 Gbps / mm <sup>2</sup>
Infobit/Cycle	0.15-1.77	0.58-6.70	0.13-0.75	3.09

# FlexiChaP configured for LDPC decoding

Flexible Channel coding Processor (FlexiTreP + LDPC functionality)

- Only reuse of memories and pipeline stages
- Two reconfigurable barrel shifters (submatrix size)



# LDPC Assembler Code

- Supports structured parity check matrices (WiMAX, WiFi, UWB)
- WiMAX source code (N=576, R=1/2) :

```
.text
l.subm 24                ; reconfigure networks and
                        ; set submatrix size to 24

l.diag 0, s=1, a=1      ; process submatrix
l.diag 0, s=6, a=2      ; s determines shift offset
l.diag 0, s=11, a=8     ; a determines address
l.diag 0, s=4, a=9
l.diag 0, s=23, a=12
l.diag 1, s=0, a=13     ; last edge of check node

l.diag 0, s=18, a=1     ; new check node begins
l.diag 0, s=19, a=5
l.diag 0, s=5, a=6
l.diag 0, s=22, a=7
l.diag 0, s=21, a=11
l.diag 0, s=0, a=13
l.diag 1, s=0, a=14     ; last edge of check node
...
l.diag 0, s=23, a=12
l.diag 1, s=0, a=23     ; last edge of check node

l.pchk it=10           ; perform parity check
nop
PD                     ; power down
```

# FlexiChaP: Synthesis Results

- LDPC Throughput: 27.7 – 257.0 Mbit/s @ 400 MHz

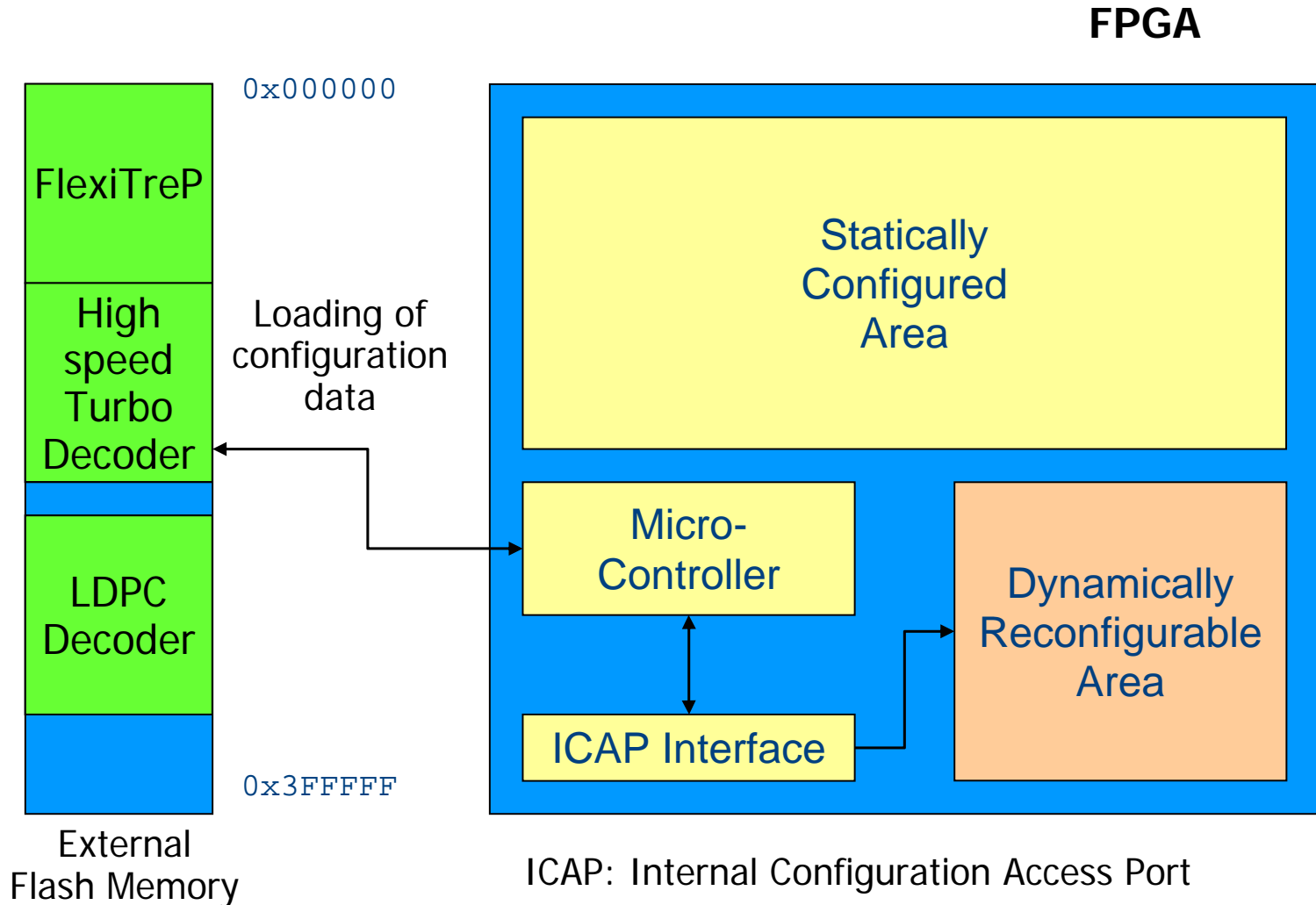
Functionality	Standard cells (65nm)		FPGA (Xilinx xc4vlx80-12)	
	Area [ $\mu\text{m}^2$ ]	Frequency [MHz]	Slices	Frequency [MHz]
FlexiTreP (CC/TC)	109320	400	7012	109
LDPC ASIP	113099	425	8076	132
FlexiChaP (CC/TC/LDPC)	232346	400	14495	109

- FlexiTreP      0.11 mm<sup>2</sup> logic + **0.31mm<sup>2</sup> memory** = 0.42mm<sup>2</sup>
- LDPC ASIP    0.11 mm<sup>2</sup> logic + **0.20mm<sup>2</sup> memory** = 0.31mm<sup>2</sup>
- FlexiChaP     0.23 mm<sup>2</sup> logic + **0.39mm<sup>2</sup> memory** = 0.62mm<sup>2</sup>
- LDPC IP Core: 0.11 mm<sup>2</sup> logic + **0.20mm<sup>2</sup> memory** = 0.31mm<sup>2</sup>

**Same size but much shorter development time for ASIP!**

# Dynamic Reconfiguration

- No reuse of logic in FlexiChaP, lack of very high-throughput
- Dynamic reconfiguration of channel decoding IPs



# First Results

<b>Xilinx xc4vlx80-12</b>	<b>LDPC IP Core</b>	<b>LDPC ASIP</b>	<b>FlexiTreP</b>	<b>FlexiChaP</b>	<b>with Dynamic Reconfiguration</b>
<b>BRAMs</b>	13	12	26	26	26
<b>Slices</b>	7135	8076	7012	14495	8000
<b>MHz</b>	203	132	109	109	109/203

## **Flexibility in several dimensions**

- IP ASIP level: software, dynamic reconfiguration
- Dynamically loadable IP decoders

## **Open Questions/Challenges**

- Time for dynamic reconfiguration ?
- Additional logic overhead ?
- SPP Partners: Prof. Teich, Prof. Becker, Prof. Glesner....

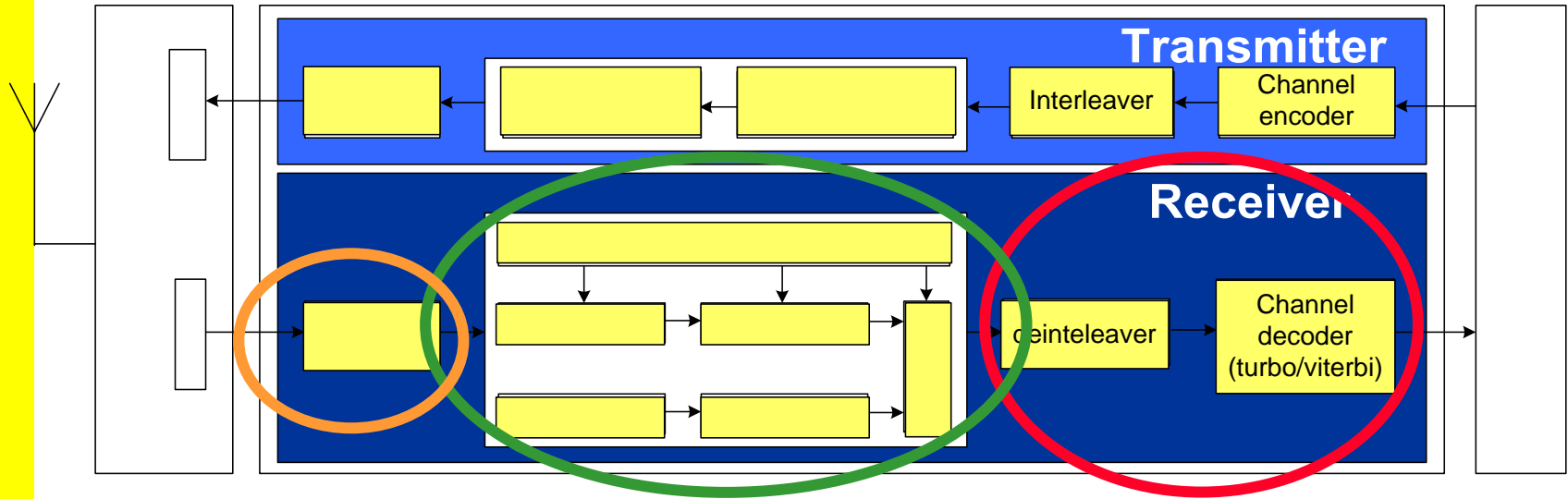
# Conclusion

- **Outer Modem in SDR**
  - **Weakly programmable IP Core**
- **IP Core based on „unlimited“ ASIP approach**
  - **Very promising results**
- **Flexibility in several dimensions**
  - **Design time configurability**
  - **Low level software programmability**
  - **Reconfigurability at run-time**
    - **Microarchitectural level**
    - **ASIP/IP Core level**

# Publications

- A Reconfigurable Application Specific Instruction Set Processor for Convolutional and Turbo Decoding in a SDR Environment T. Vogt, N. Wehn. *IEEE Conference Design, Automation and Test in Europe (DATE '08)*, March 2008, Munich, Germany.
- Flexibility/Reconfigurability Trade-offs in SDR Architectures N. Wehn. *Workshop Reconfigurable Computing - IEEE Conference Design, Automation and Test in Europe (DATE '08)*, March 2008, Munich, Germany.
- Proving Functional Correctness of Weakly Programmable IPs - A Case Study with Formal Property Checking S.Loitz, M.Wedler, C.Brehm, T.Vogt, N.Wehn, W.Kunz. *Accepted for publication, IEEE Symposium on Application Specific Processors (SASP 2008)*, June 2008, Anaheim California, USA.

# UMTS/W-CDMA Physical Layer



Source: Scott Mahlke / MPSoC'06

**Filtering** Suppress signals outside frequency band

**(De)Modulation** Map signal waveforms onto symbols

**Channel Estimation** Estimates channel condition for transceivers

**Channel Decoding** Correct errors induced by noisy channel

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