

Entwurf und Optimierung heterogener ASIP / eFPGA (rASIP) - Architekturen

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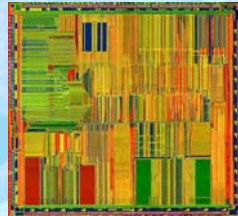


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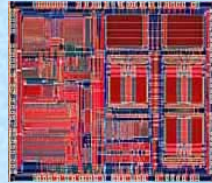


- ❑ **Motivation**
- ❑ **Arithmetikorientierte eFPGAs**
 - ▶ **Architektur-Template**
 - ▶ **Entwurfsablauf**
 - ▶ **Mathematische Modellbildung**
 - ▶ **Parameteroptimierung**
- ❑ **ASIP-eFPGA-Architekturen**
 - ▶ **ASIP Entwurfsablauf**
 - ▶ **Kopplungsmodi**
 - ▶ **Strukturelemente zur Kopplung**
 - ▶ **Abbildung exemplarischer Anwendungen**
- ❑ **Zusammenfassung**

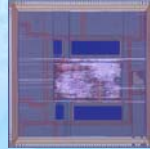
Range of Implementation Styles



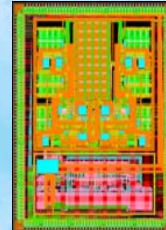
GPP



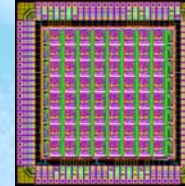
DSP



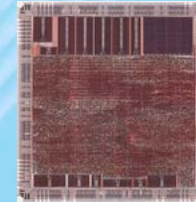
ASIP



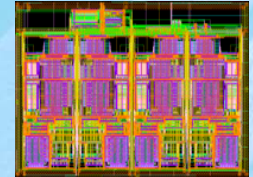
FPGA w/
Hardcore



FPGA



Standard
Cell

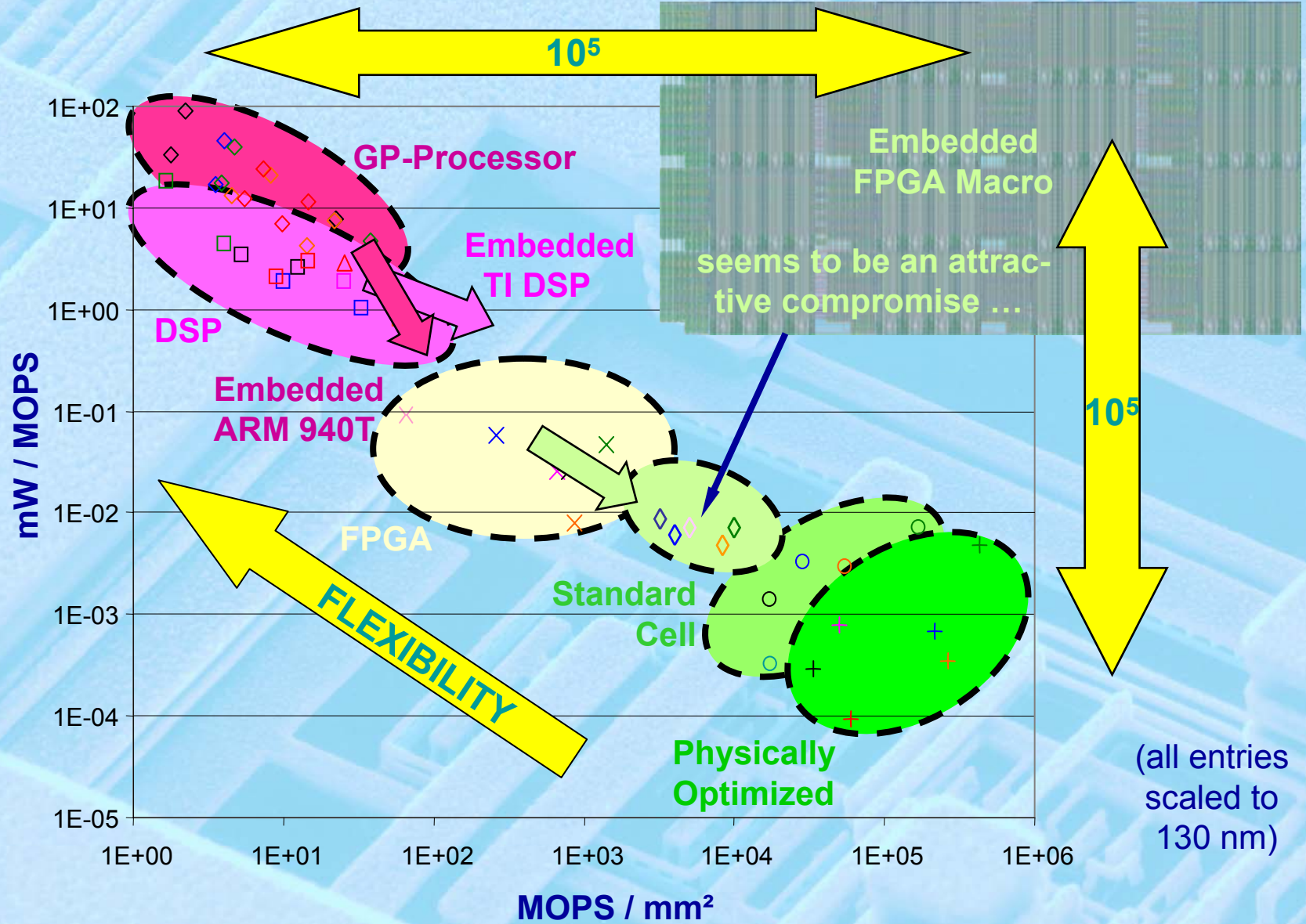


Physically
Optimized

← Increasing flexibility

→ Increasing energy & area efficiency

Motivation: Closing the Efficiency Gap

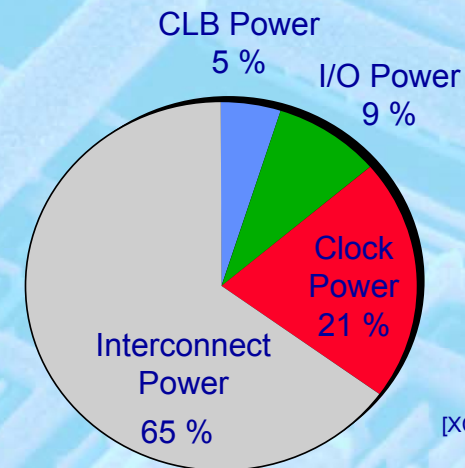


Eigenschaften Arithmetik

- ❑ Iterativ ... 2D Bit-Slice / Function-Slice Struktur
- ❑ Wenige, einfache Basisoperationen ... optimierte LUTs
- ❑ Regulär ... Shared SRAMs
- ❑ Inhärent lokal ... dedicated interconnects (local / broadcast) ...

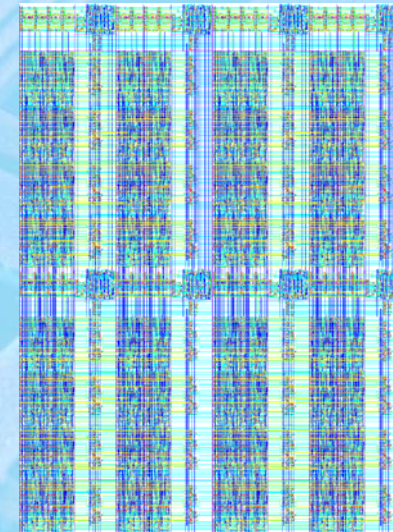
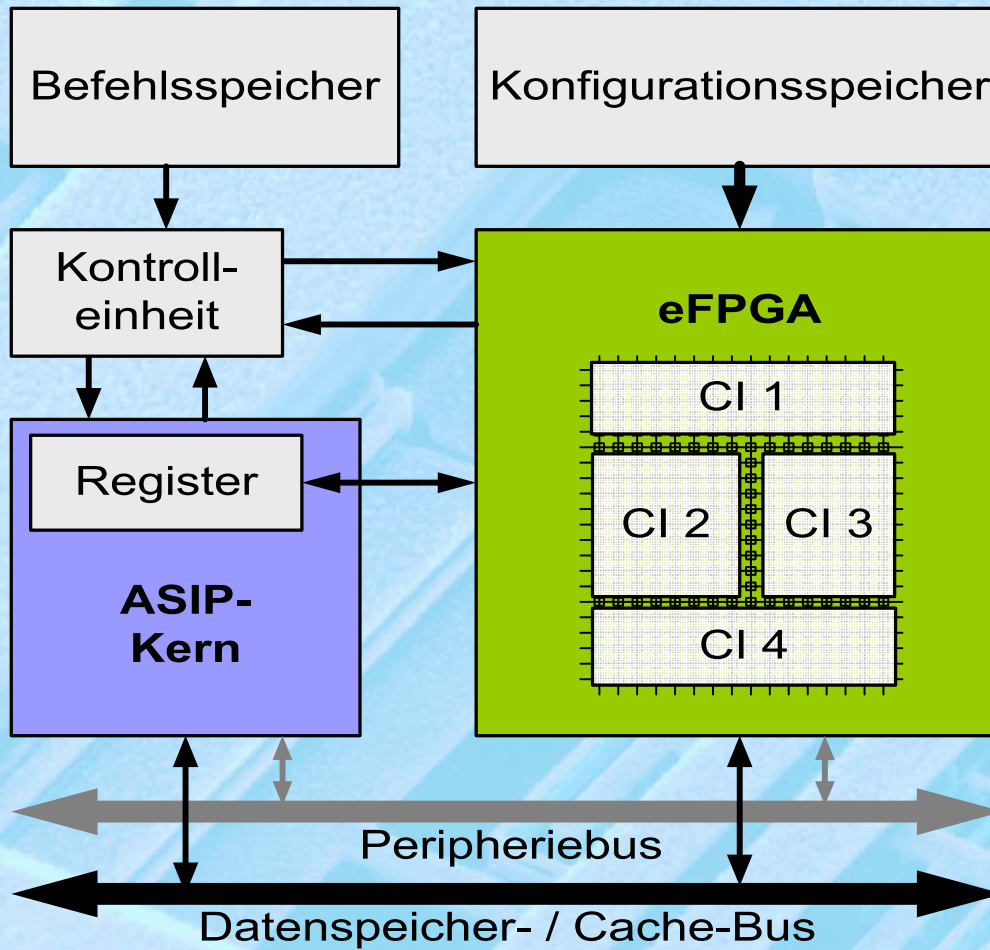
⇒ **Bessere Effizienz für Arithmetik**

⇒ **Volle Flexibilität, aber ...**



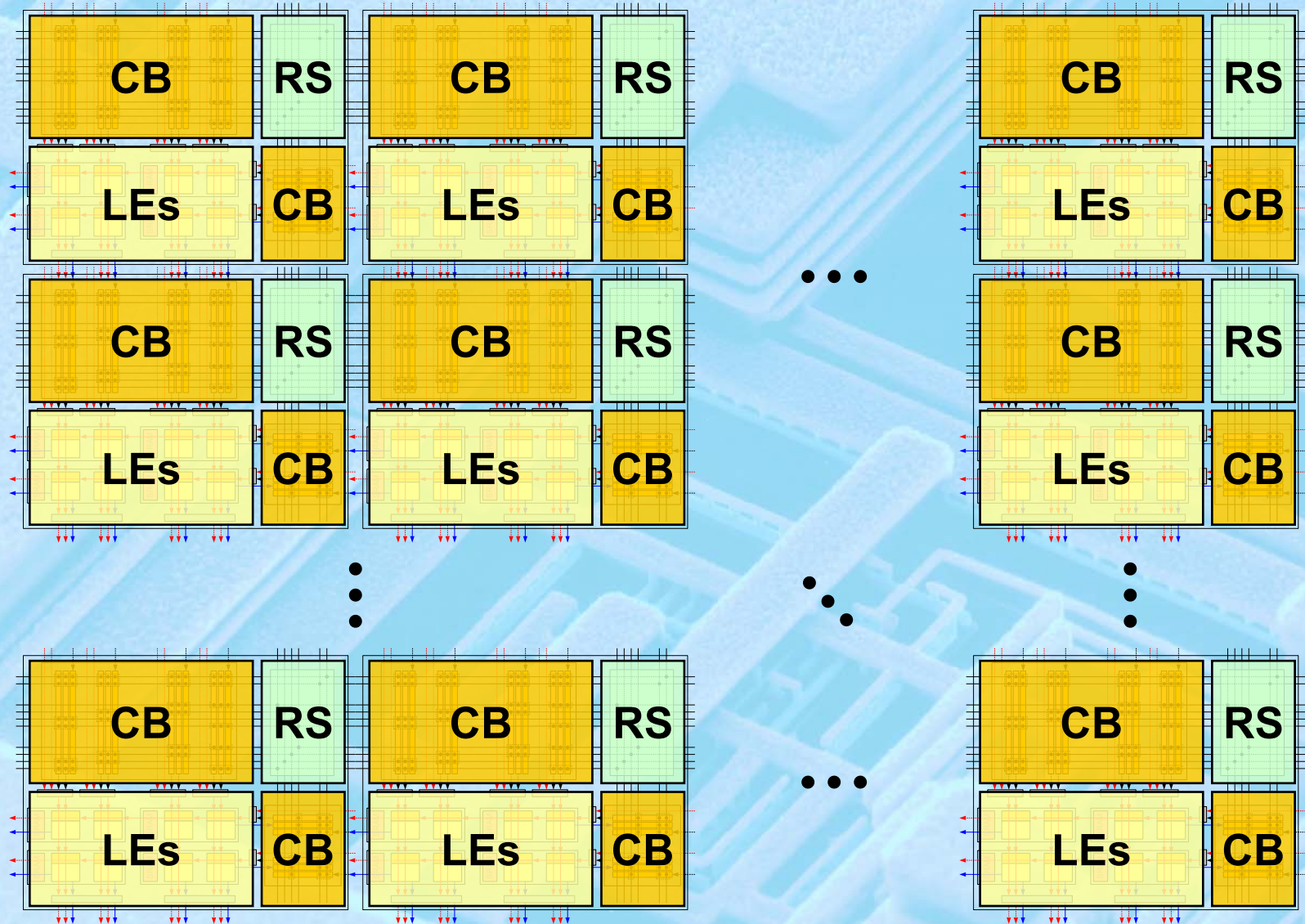
[XC4003, Kusse'97]

Motivation rASIP

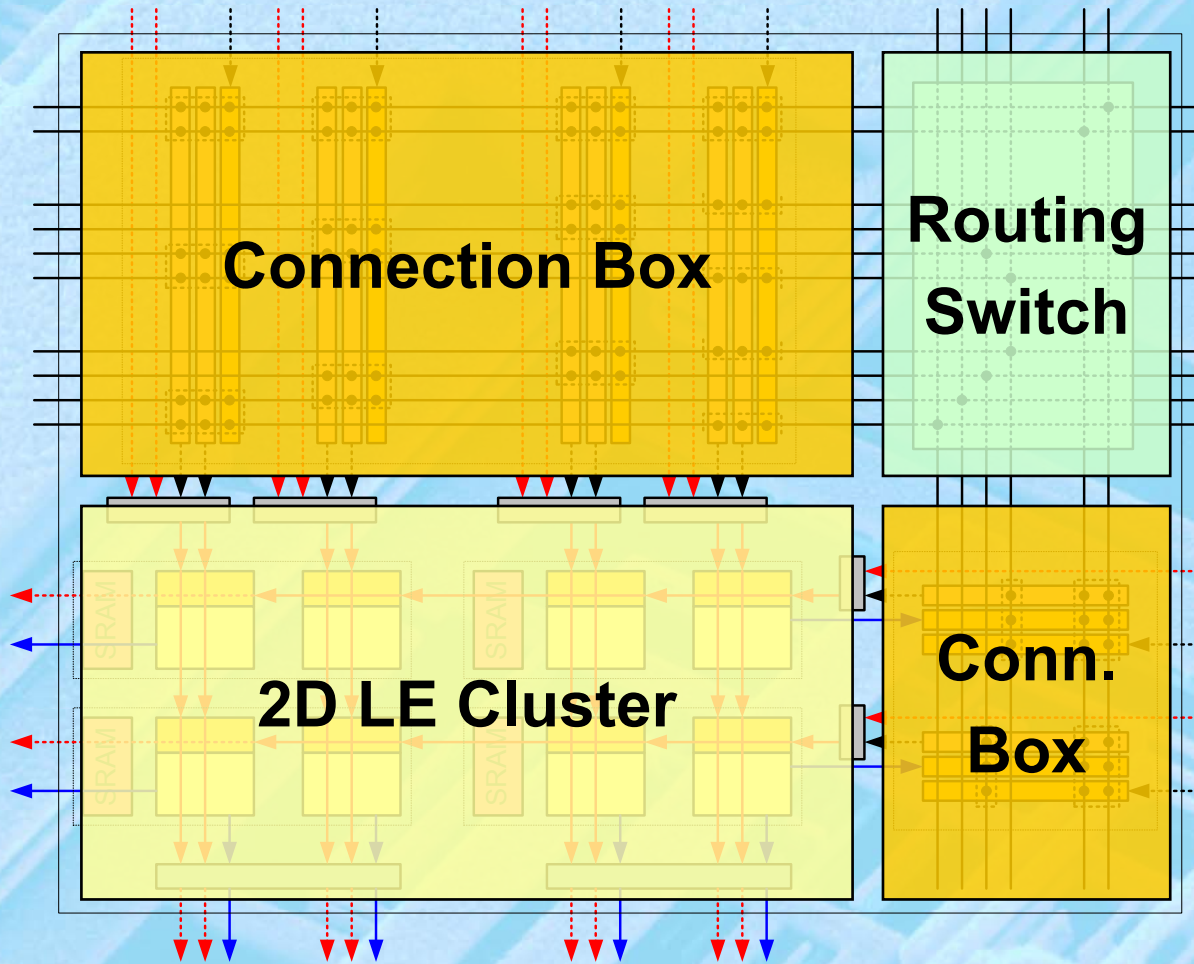


- 64 LEs
- 90 nm CMOS
- 6 basic cells
- 82928 xtrs
- 89466 μm^2

eFPGA: Architektur-Template



Architektur-Template



❑ Cluster:

- # LEs (hor. / ver.)
- # Broadcast-Ltg.
- # Shared SRAMs
- E/A Richtungen

❑ Logikelement:

- Funktionalität (Kernlogik)
- Konnektivität (DRB)

❑ Registerstufe:

- # LEs (Spalte) pro Reg.
- # LE Ausgänge mit Reg.
- Typ (Register, Latch, ...)

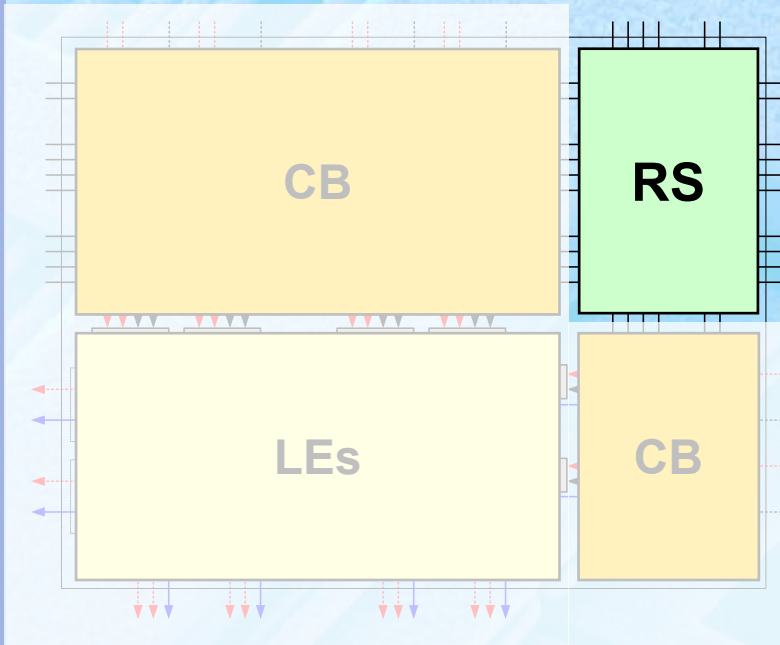
❑ Routing Switch:

- # Leitungen
- Switch Point Positionen
- Switch Point Konnektivität
- # Shared SRAMs
- Segmentlängen

❑ Connection Box:

- # Ltg. pro Gruppe
- Fenstergröße
- Fenstergeschwindigkeit
- Fensterphase
- Fensterperiodizität
- # Shared SRAMs

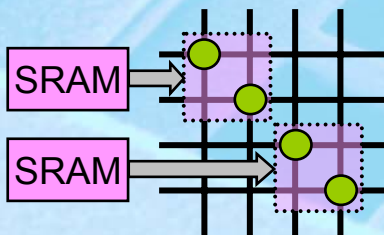
Architektur-Template: RS Parameter



z.B. Routing Switch

- # Leitungen
- Switch Point Positionen
- Switch Point Konnektivität
- # Shared SRAMs
- Segmentlängen

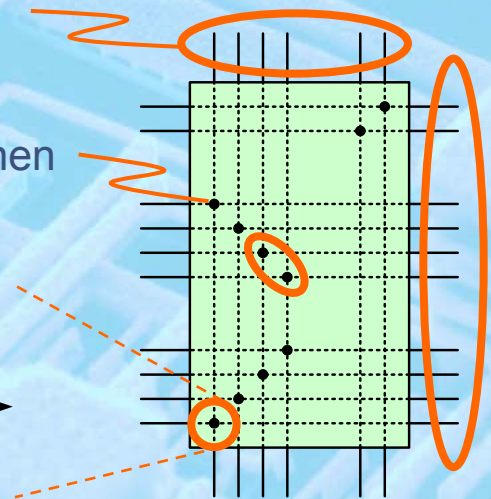
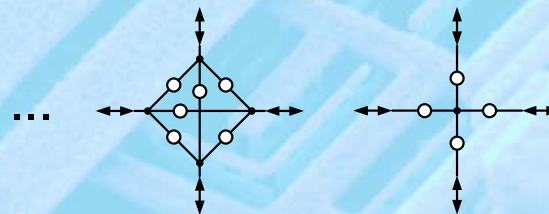
Shared SRAMs



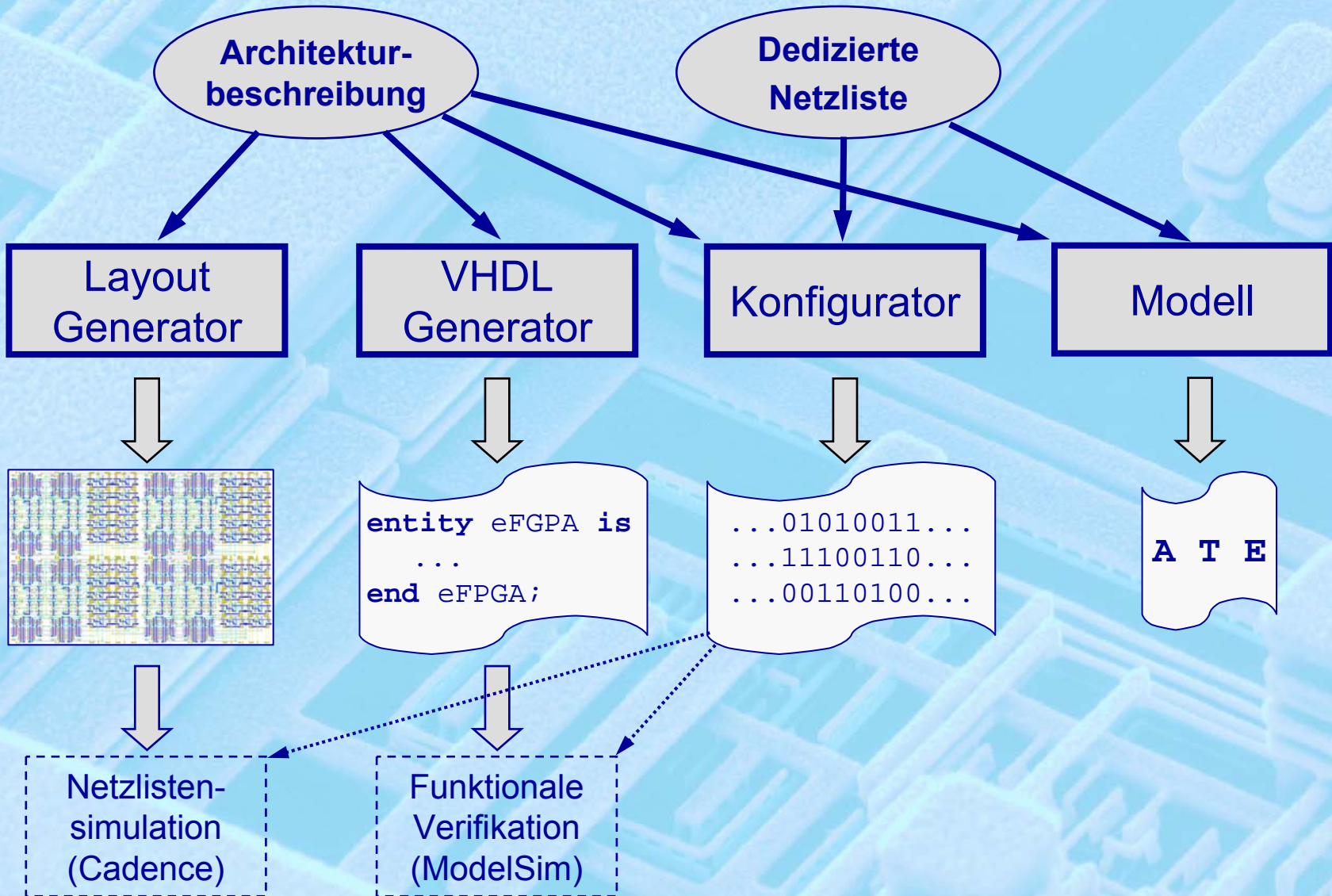
Leitungen

SP Positionen

SP Konnektivität

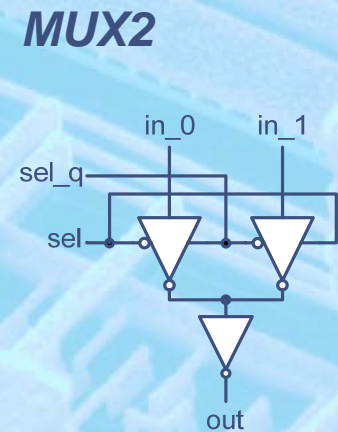
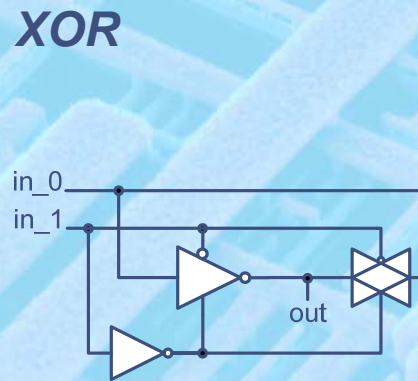
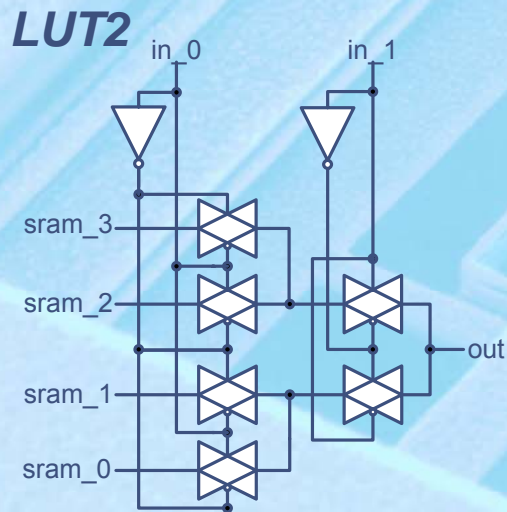
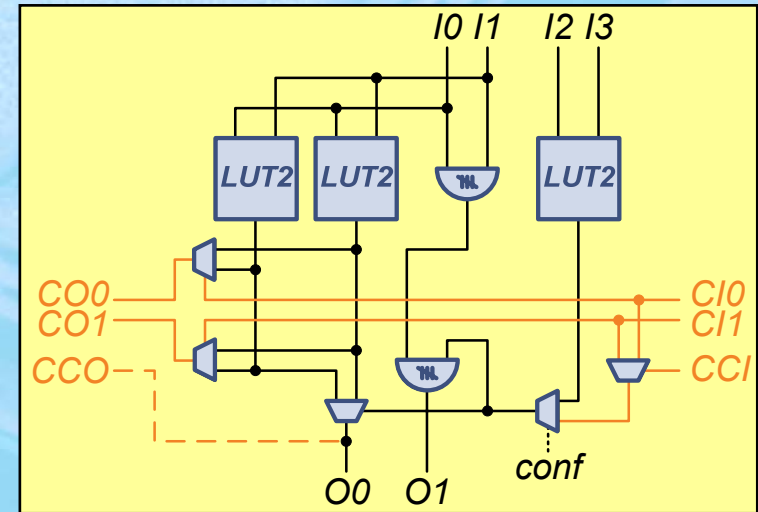
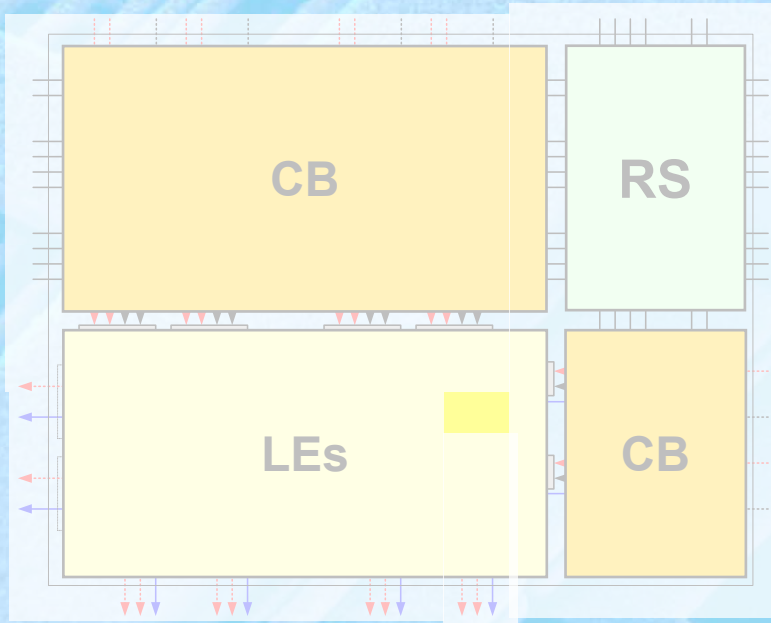


Entwurfsablauf



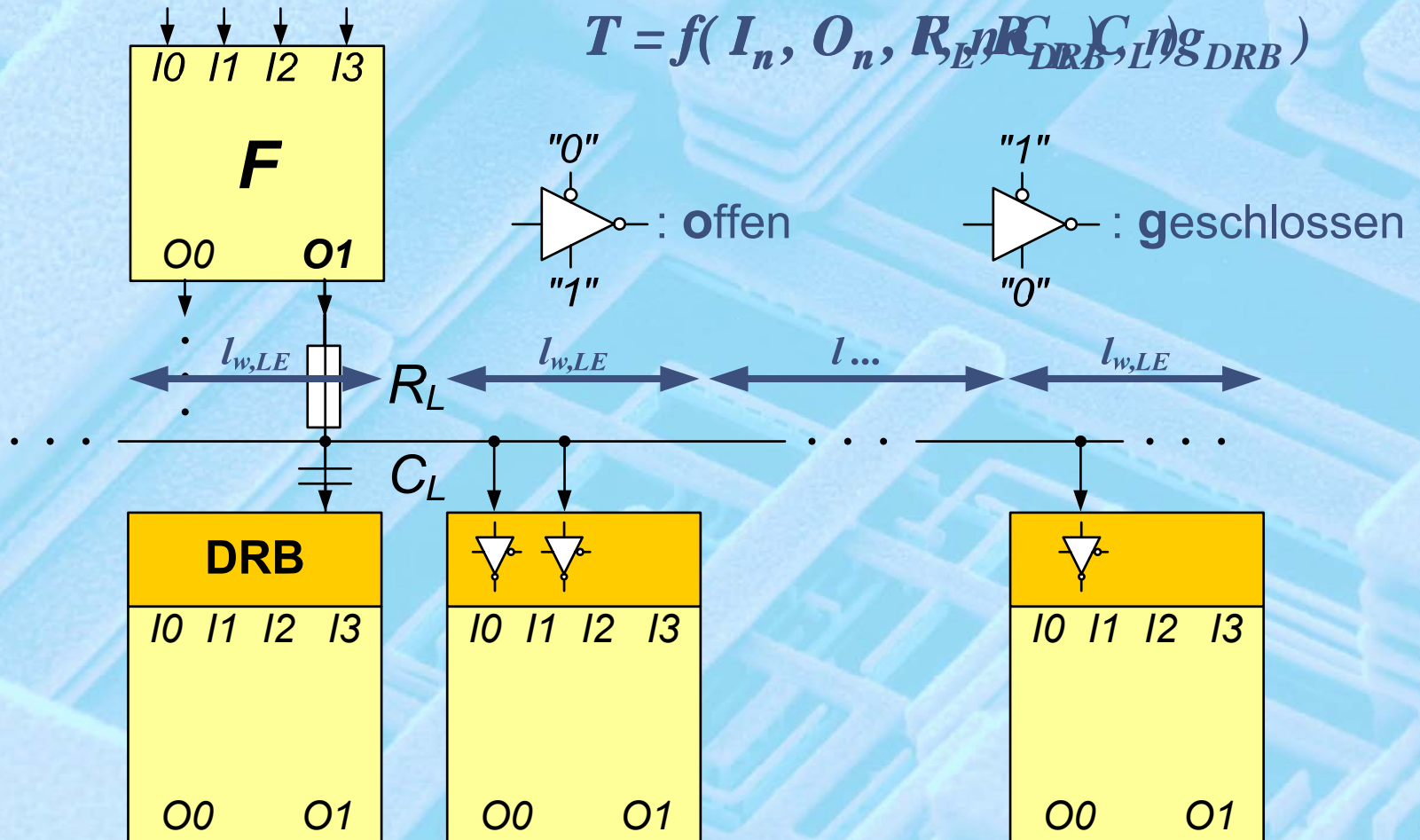
- ❑ Implementierung der Basiszellen
 - ▶ Dimensionierung (iterativ)
 - optimiert hinsichtlich P_V
- ❑ Spezifische Netzlistensimulationen
- ❑ Charakterisierung
- ❑ Modellgleichungen für A , T , E
- ❑ ATE-Gesamtmodell

Modellbildung: Kernlogik

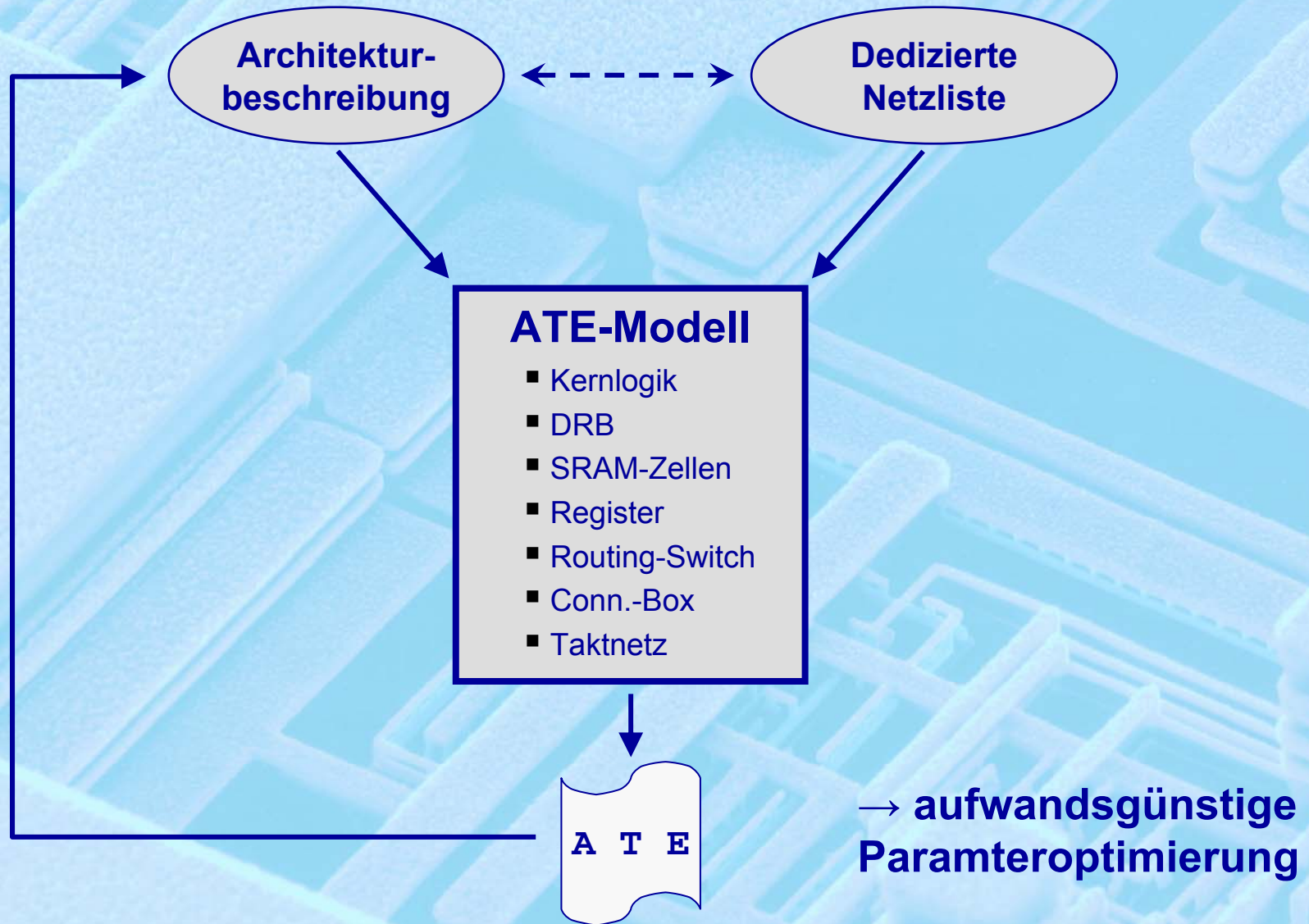


Modellbildung: Modellgleichungen

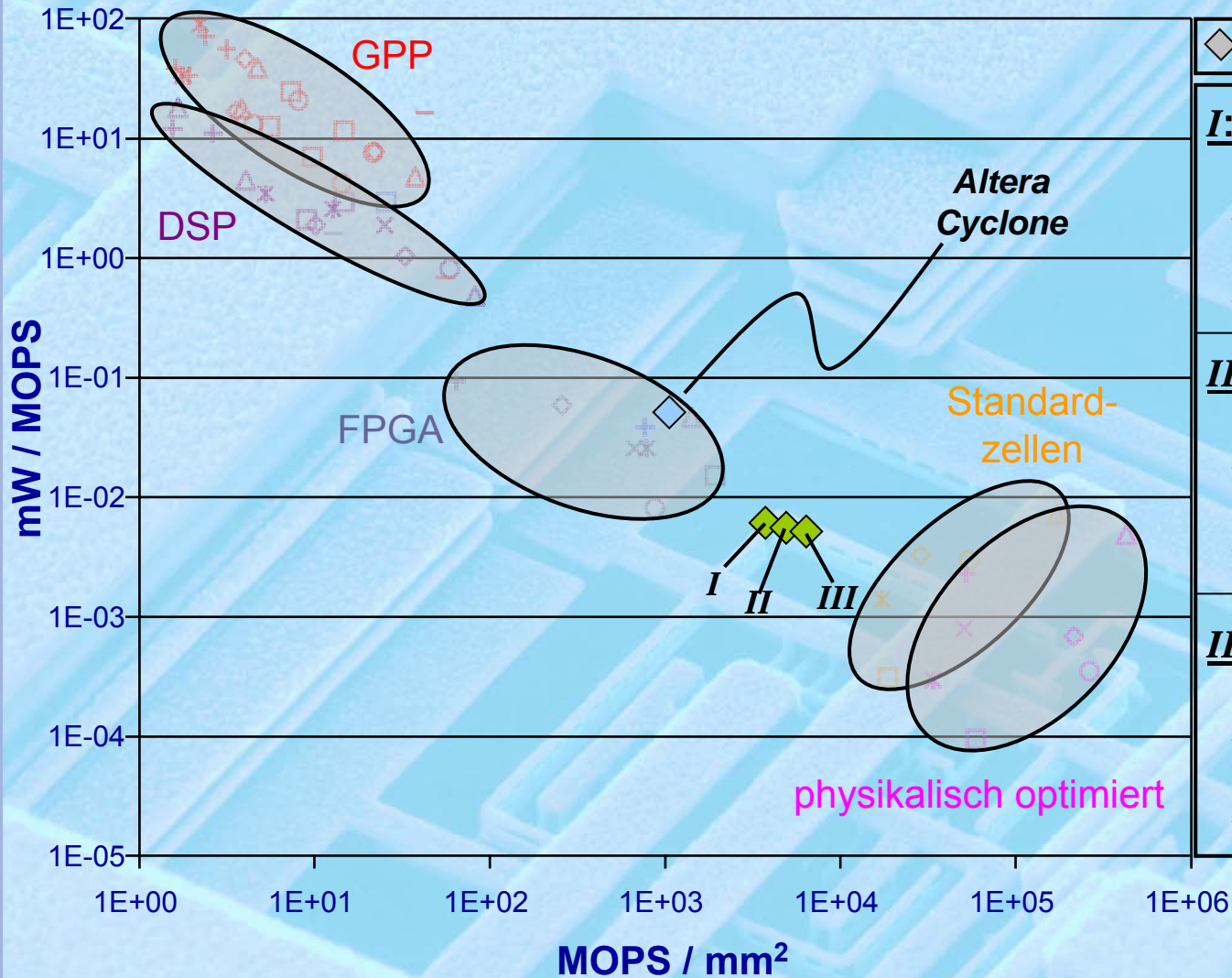
z.B. Signallaufzeit Kernlogik:



Modellbildung: ATE-Modell



Parameteroptimierung



◆ 4-tap 1D-FIR-Filter

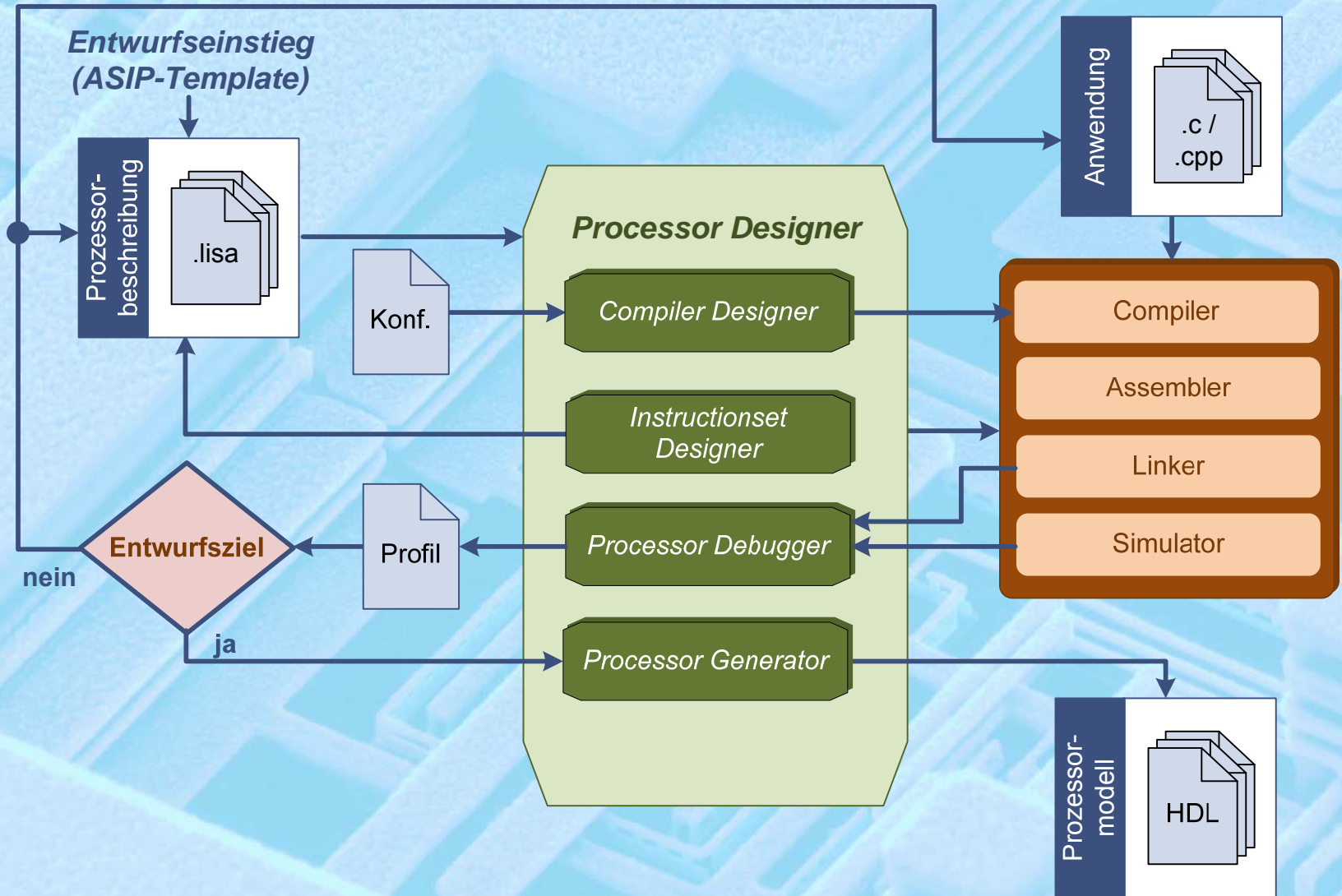
I:
 $C_H = C_V = 4$
 $M_{LE} = 2, M_{CB} = 1, M_{RS} = 4$
 $W_H = W_V = 8$
 $N_{Reg} = 2$

II:
 $C_H = 8, C_V = 4$
 $M_{LE} = 8, M_{CB} = 1, M_{RS} = 2$
 $W_H = 8, W_V = 4$
 $N_{Reg} = 2$

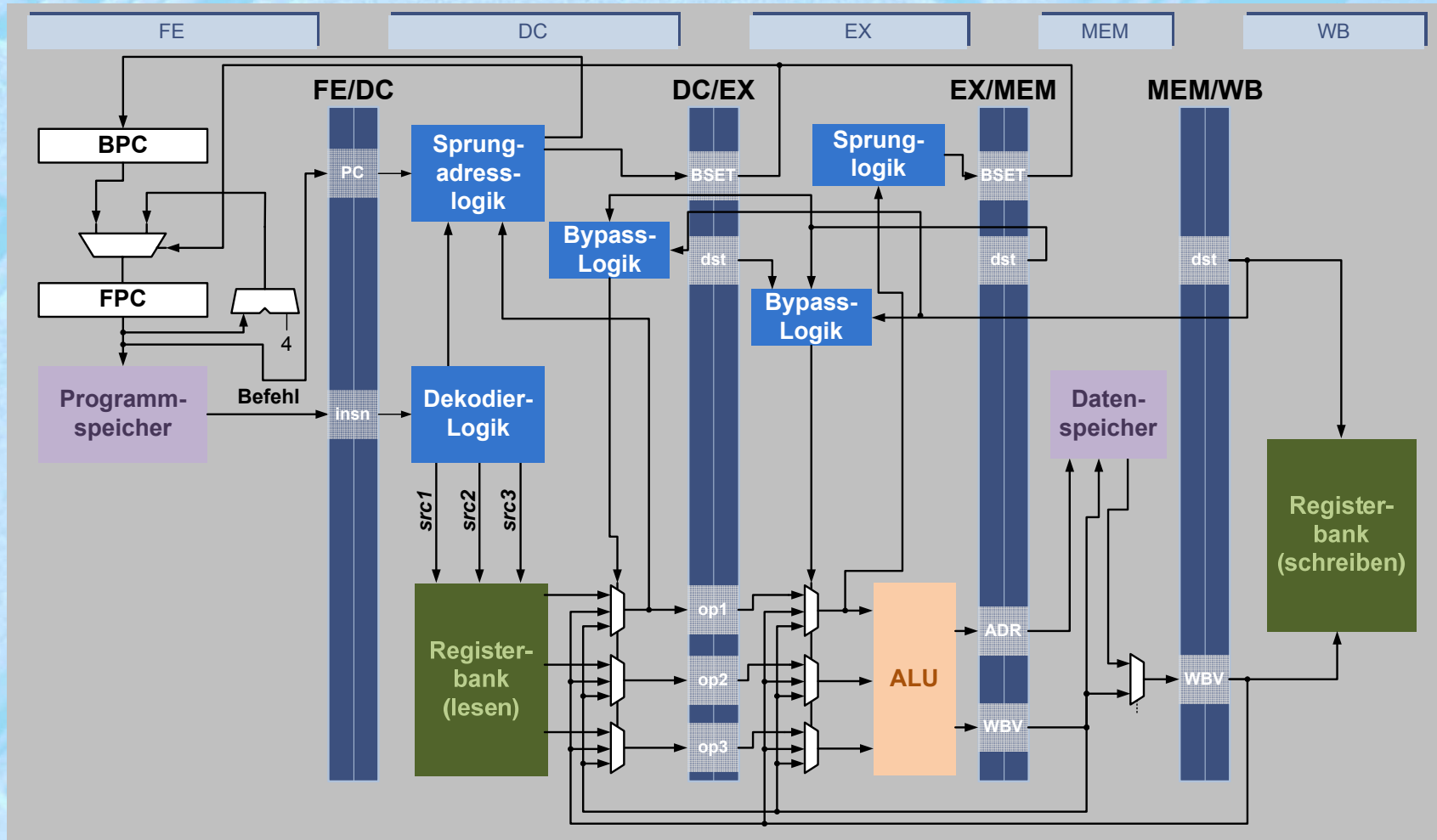
III:
 $C_H = 16, C_V = 4$
 $M_{LE} = 16, M_{CB} = 1, M_{RS} = 4$
 $W_H = W_V = 8$
 $N_{Reg} = 2$



ASIP Entwurfsablauf



ASIP-Template (LT_RISC)



- ❑ 5-stufige Pipeline
- ❑ 16 Register

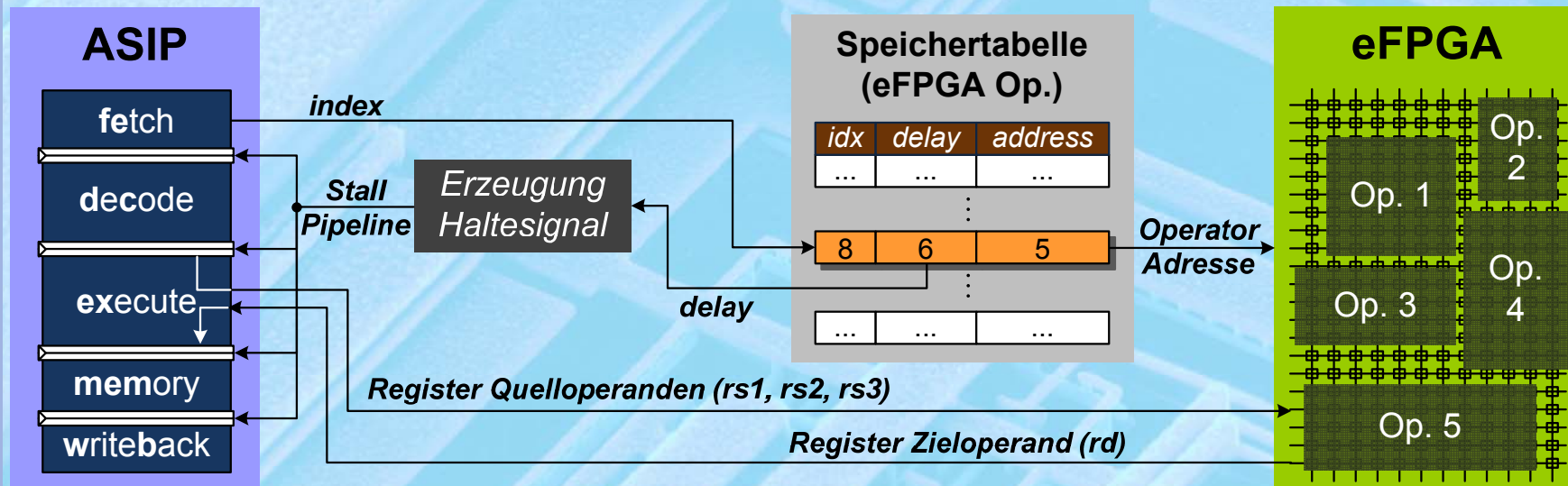
- ❑ 32-bit Datenpfad
- ❑ RISC-Befehlssatz

Kopplungsmodi

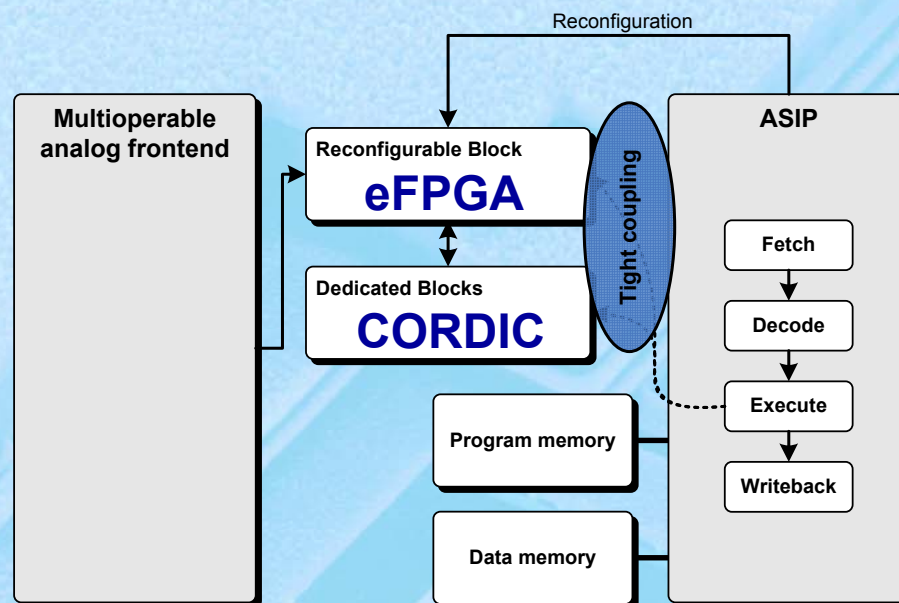
Kopplungsmodus	Komplexität der ausgelagerten Operationen	Datenkommunikation	Synchronisation (ASIP-eFPGA)
<i>TC</i>	niedrig	Registerbank	Anhalten der ASIP-Pipeline
<i>LC</i>	hoch	Registerbank	Interrupt-Mechanismus
<i>LC-MEM</i>	hoch	Datenspeicher	Interrupt-Mechanismus
<i>hybrid</i>	variabel	Registerbank / Datenspeicher	Anhalten der ASIP-Pipeline / Interrupt-Mechanismus

Strukturelemente zur Kopplung

CI: `efpga_ci <index>,<rd>,<rs1>,<rs2>,<rs3>`



Digitales Empfangs-Makro für Multioperable GNSS



- (Very) low power
- Low- (better no-) cost
- High performance
- High flexibility

Abbildung exemplarischer Anwendungen

GPS-Empfängerarchitektur:

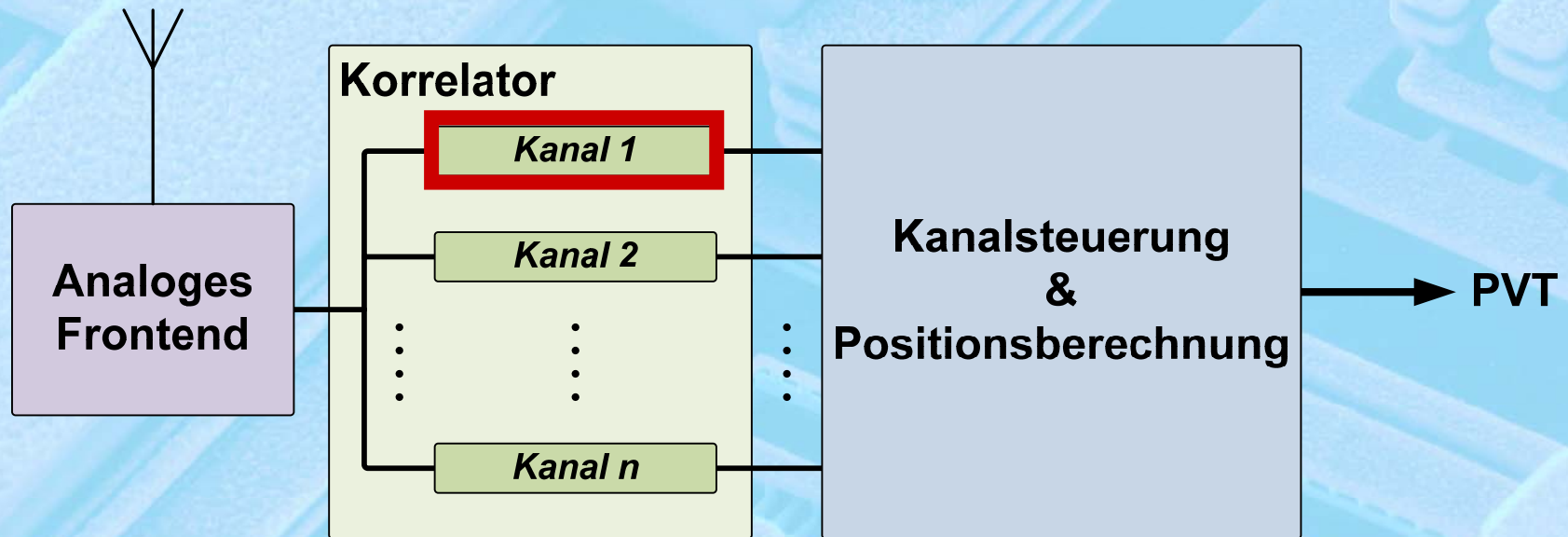
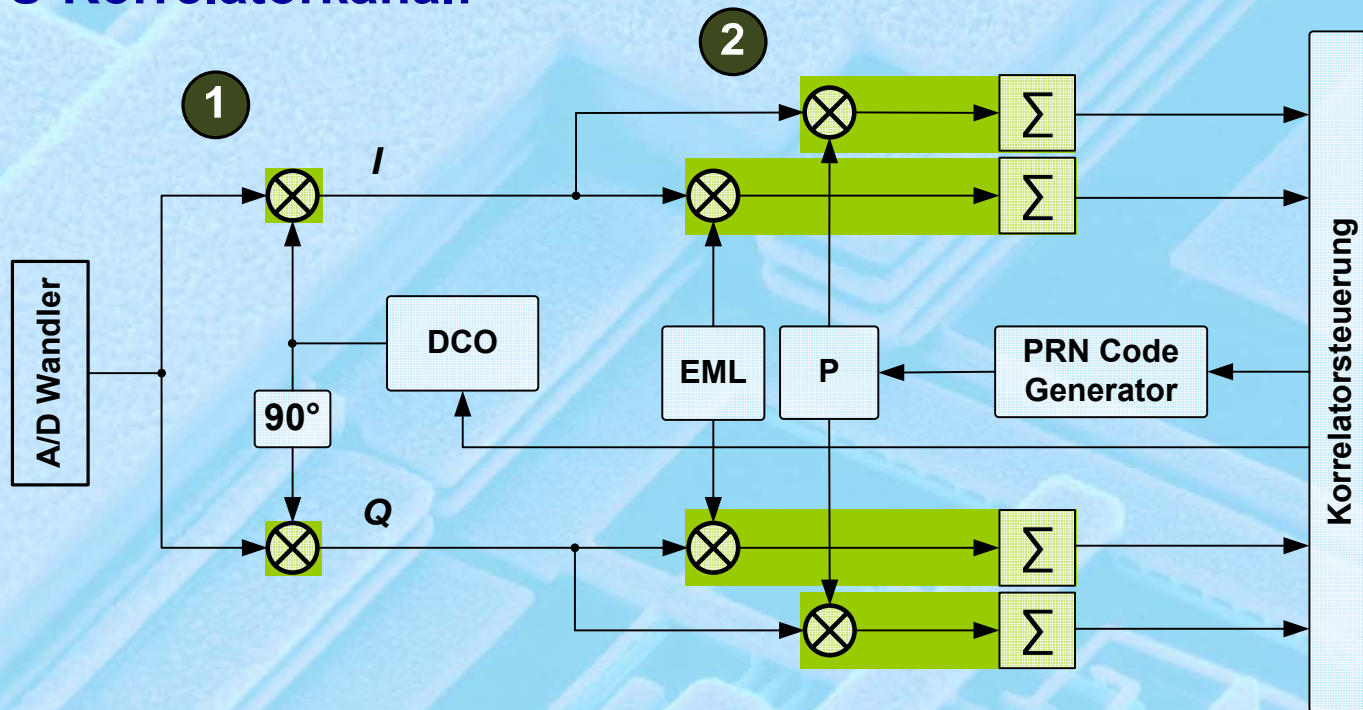


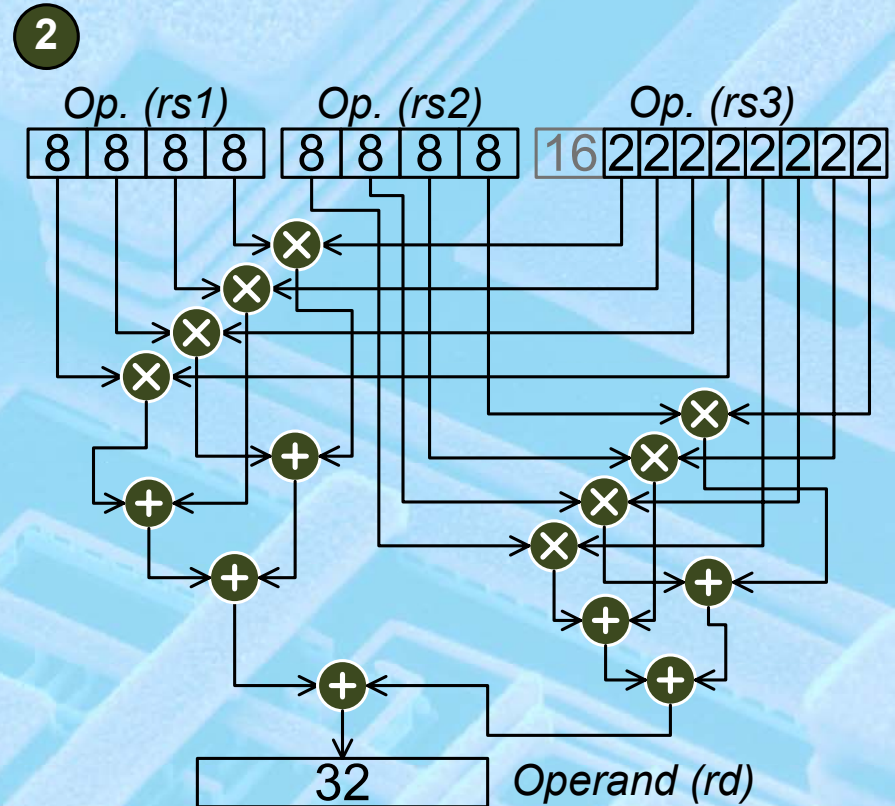
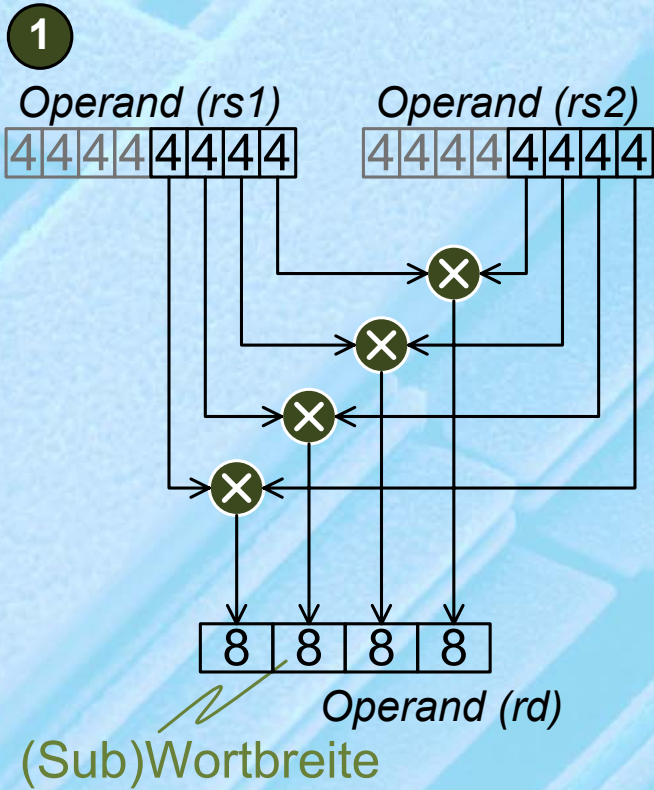
Abbildung exemplarischer Anwendungen

GPS-Korrelatorkanal:

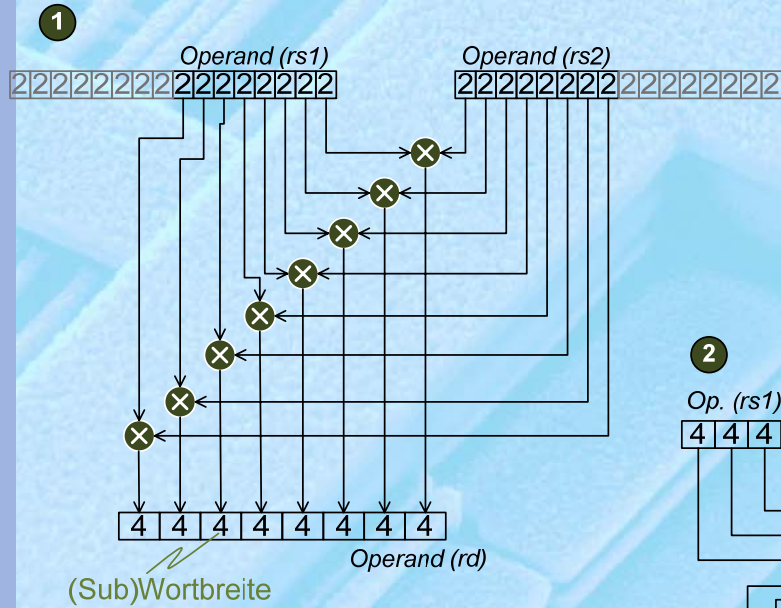


- ❑ Variable Anzahl der Kanäle
- ❑ Dynamisch adaptierbare Wortbreiten
→ Empfindlichkeit, Akquisitionszeit
- ❑ Reguläre Operationen → eFPGA
- ❑ Realisierung auf eFPGA: parallelisierbar, flexibel

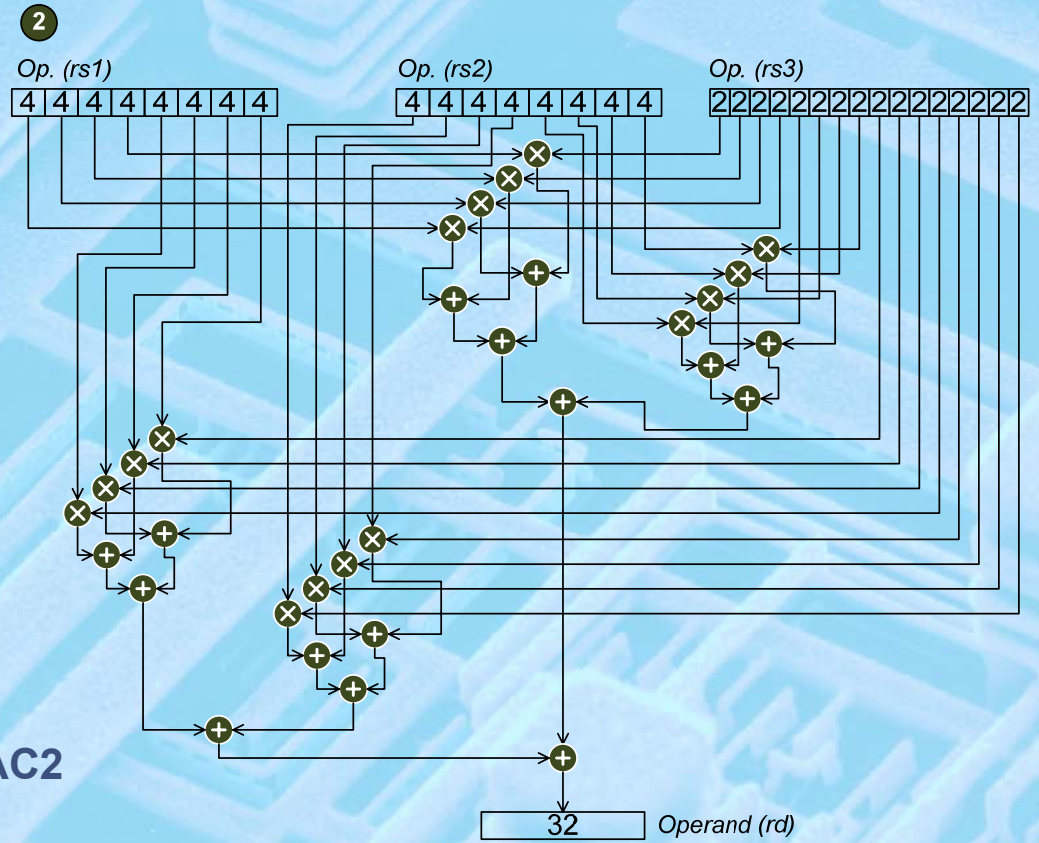
eFPGA-Operatoren (HP)



eFPGA-Operatoren (LP)

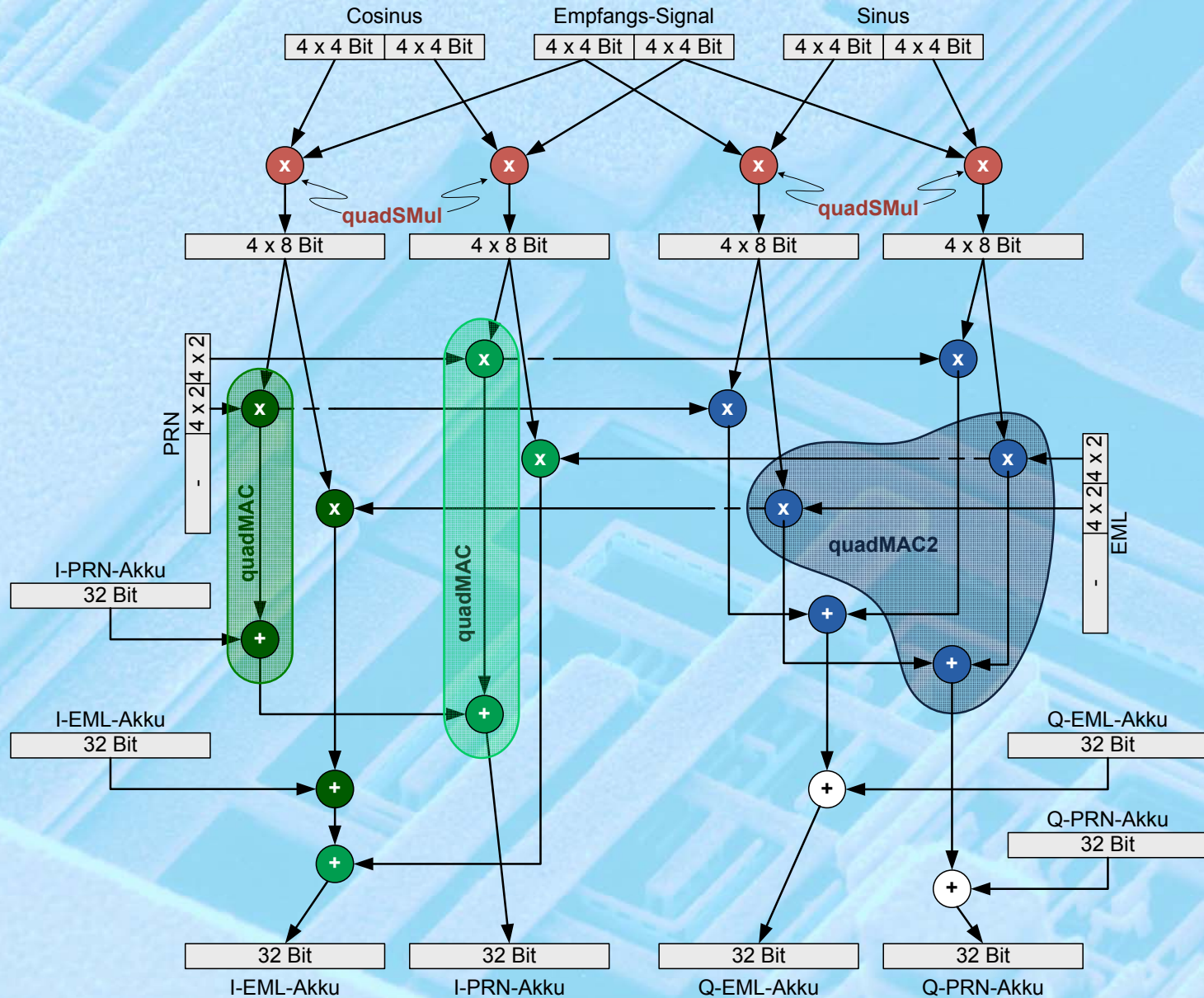


oktaSMul

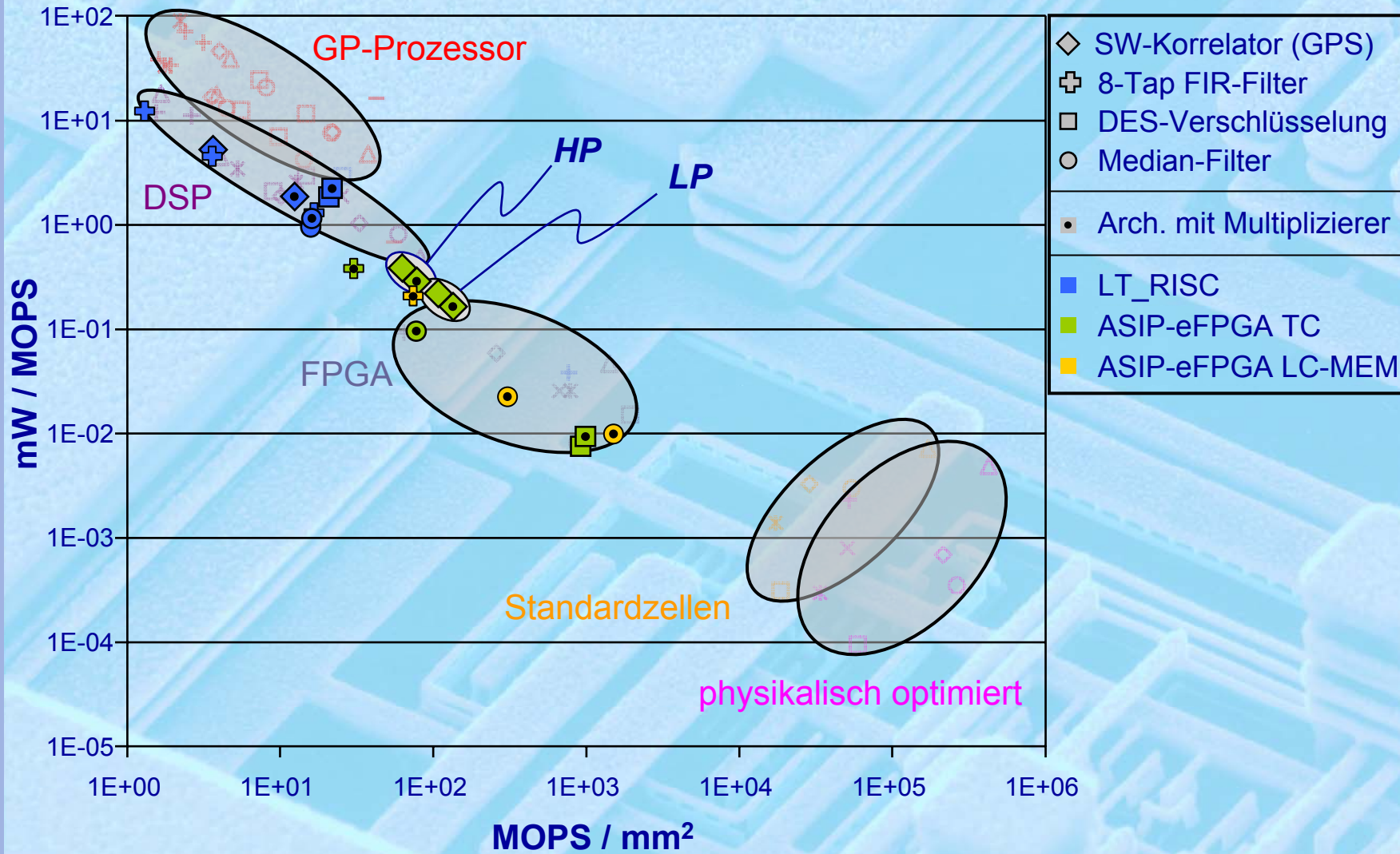


oktaMAC2

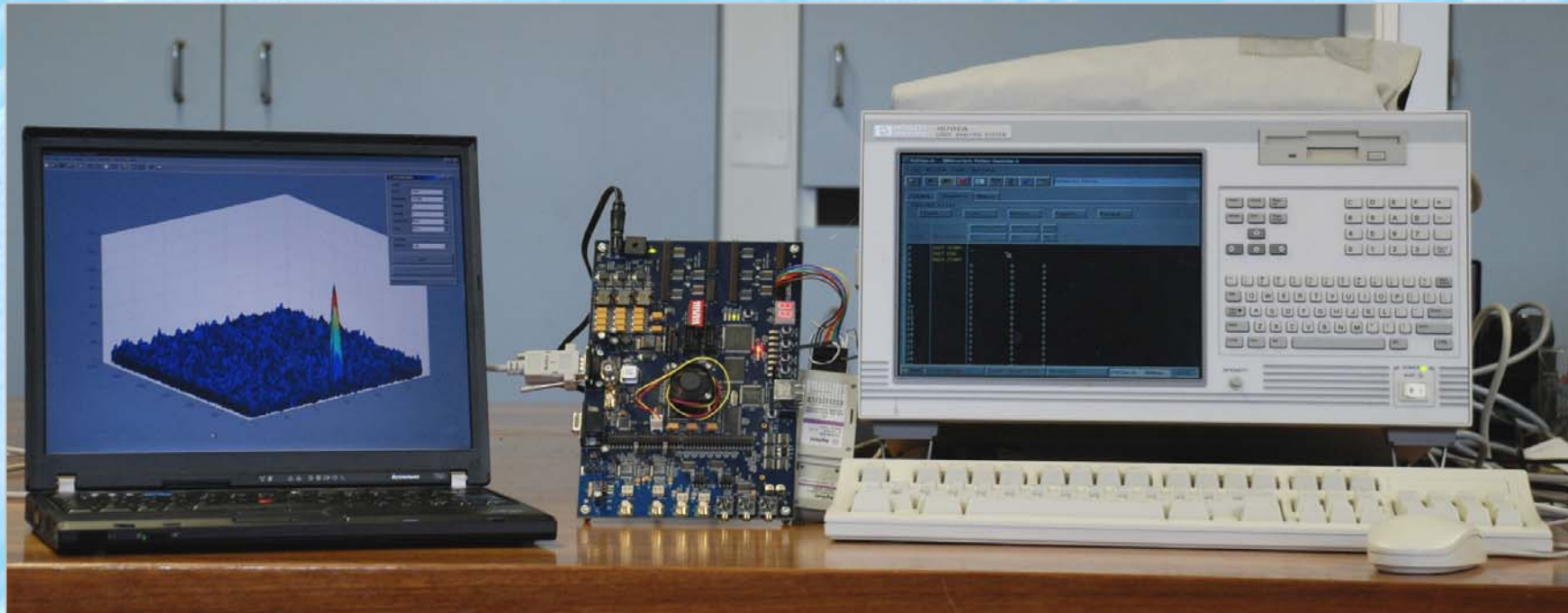
eFPGA-Operatoren (CI) — SFG (HP)



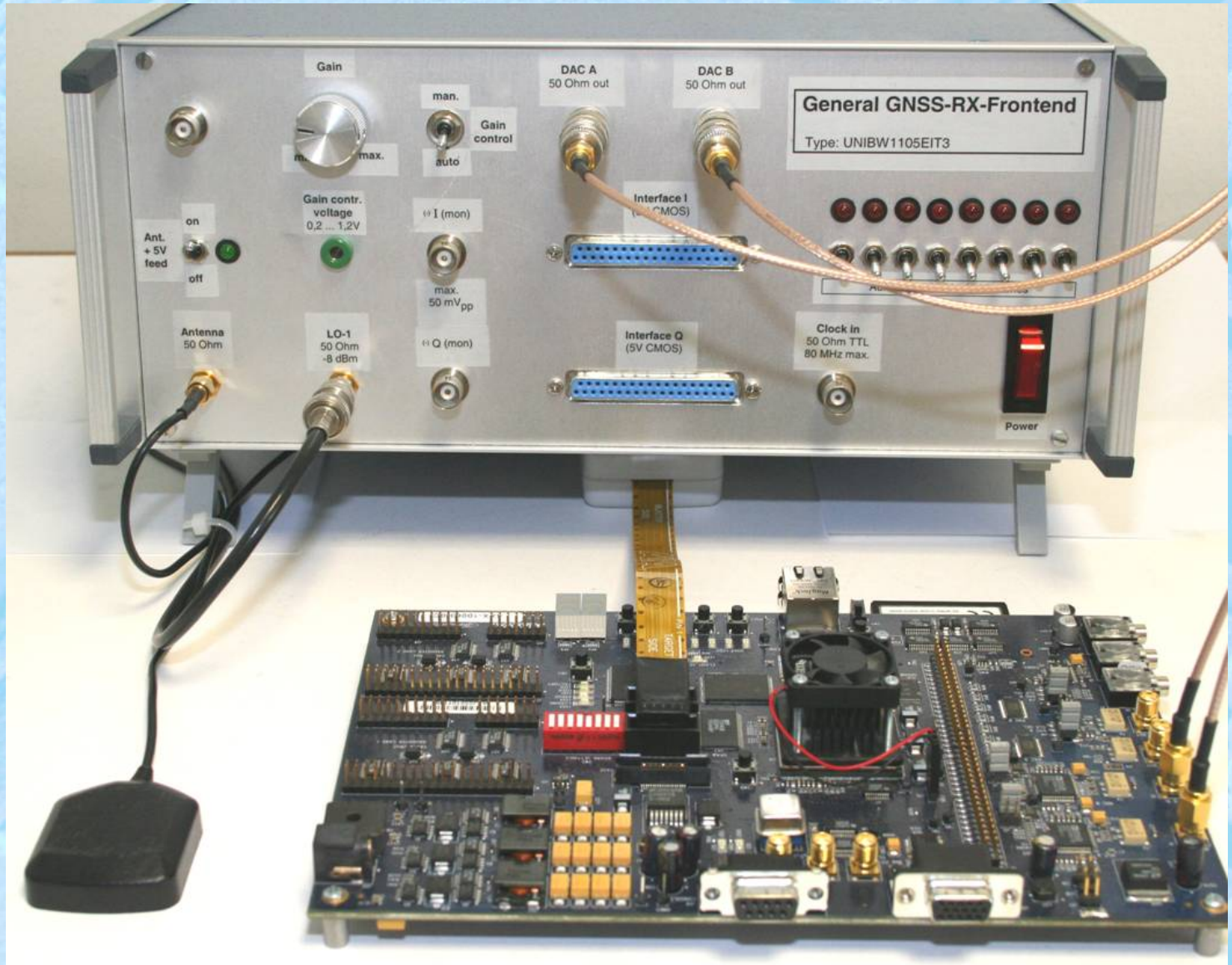
Einordnung in den Entwurfsraum



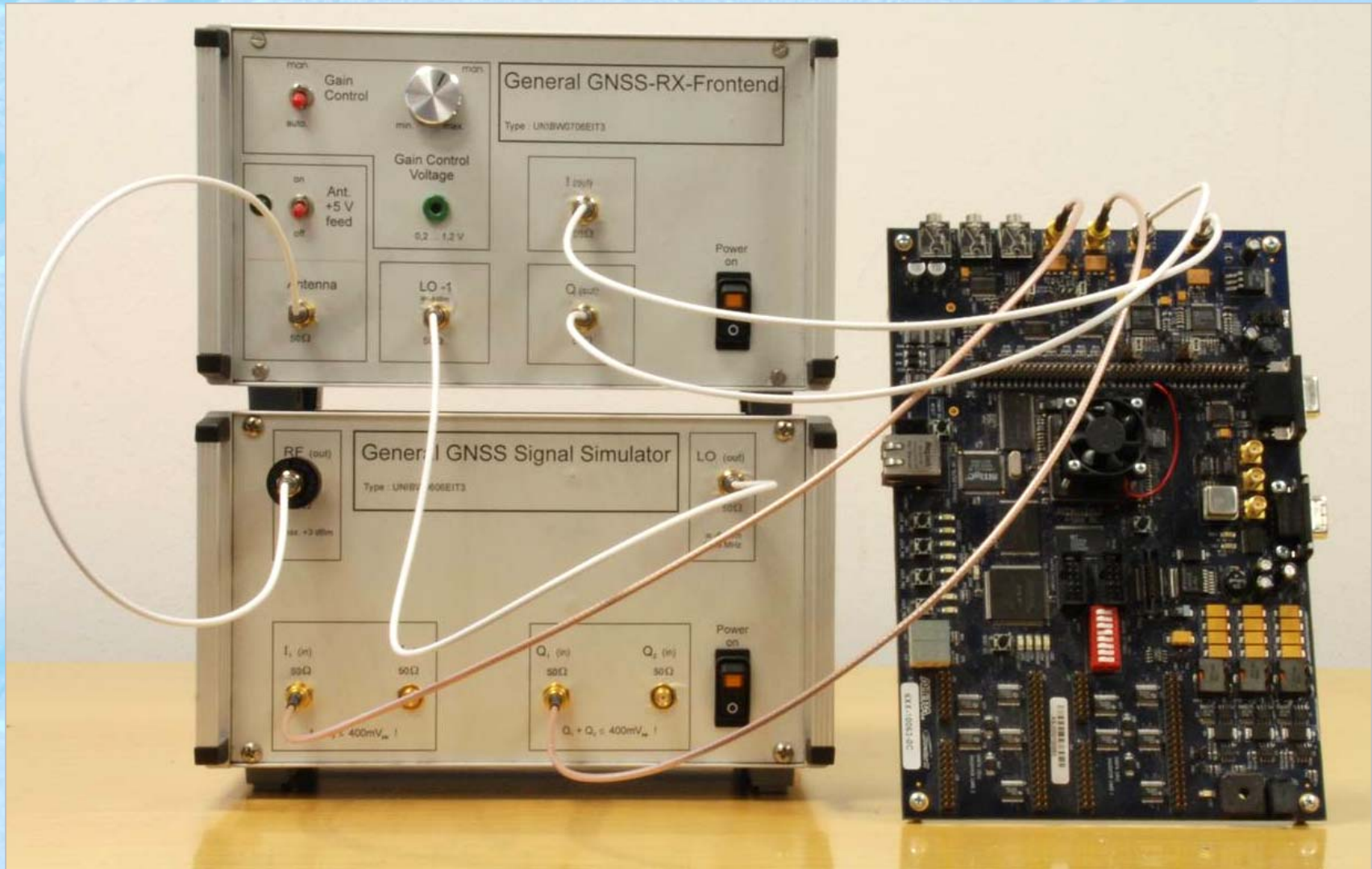
GNSS Testbeds



GNSS Testbeds



GNSS Testbeds



- ❑ **Arithmetik-orientierte eFPGAs**
 - ▶ **Enhanced Design Flow**
 - **vergleichbar DPG Approach**
 - ▶ **Modellbildung**
 - **aufwandsgünstige Parameteroptimierung**

- ❑ **ASIP-eFPGA-Architekturen**
 - ▶ **Kopplungsmodi**
 - **Effizienzsteigerung durch Wahl des Kopplungsmodus**

- ❑ **Exemplarische Anwendung**
 - ▶ **Multioperabler GPS-Empfänger**
 - **Effizienzgewinn**

Veröffentlichungen

- Neumann, B.; von Sydow, T.; Blume, H.; Noll, T. G.: *"Entwurf und quantitative Analyse parametrisierbarer eFPGA-Architekturen für Arithmetik-Anwendungen"*, Tagungsband der URSI Kleinheubacher Tagung 2005, Sep. 2005, Miltenberg
- Kappen, G.; Noll, T. G.: "Application Specific Instruction Processor Based Implementation of a GNSS Receiver on an FPGA", Proceedings of the DATE'06, 2006, München
- von Sydow, T.; Neumann, B.; Noll, T. G.: "Quantitative Analysis of embedded FPGA Architectures for Arithmetic", Proc. of the ASAP 2006, Colorado, Sep. 2006
- von Sydow, T.; Korb, M.; Neumann, B.; Blume, H.; Noll, T. G.: "Modelling and Quantitative Analysis of Coupling Mechanisms of Programmable Processor Cores and Arithmetic Oriented eFPGA Macros", Proc. of the ReConFig'06, Sep. 2006, San Luis Potosi, Mexico,
- Neumann, B.; von Sydow, T.; Noll, T. G.: "Application Domain Specific Embedded FPGAs for Flexible ISA-Extension of ASIPs", invited Paper, JVSPS 2008
- von Sydow, T.; Neumann, B.; Noll, T. G.: "Design and quantitative analysis of ASIPs with eFPGA-based accelerators as flexible ISA-extension", PhD-Forum, DATE, 2007



Veröffentlichungen (cont'd)

- Kappen, G.; el Bahri, S.; Priebe, O.; Noll, T. G.: "Evaluation of a tightly coupled ASIP / Co-Processor Architecture used in GNSS receivers", Proc. ASAP, 2007, Montreal, Canada
- Kappen, G.; Kurz, L.; Noll, T. G.: "Comparison of ASIP and Standard Microprocessor Based Navigation Processors", Proc. TimeNav, 2007, Geneva, Switzerland
- Zipf, P.; Hinkelmann, H.; Deng, L.; Glesner, M.; Blume, H.; Noll, T. G.: "A Power Estimation Model for an FPGA-based Softcore Processor", Proc. FPL, 2007, Amsterdam, Niederlande
- Neumann, B.; von Sydow, T.; Blume, H.; Noll, T. G.: "Design flow for embedded FPGAs based on a flexible architecture template", Proc. of DATE'08, 2008, München
- von Sydow, T.; Blume, H.; Kappen, G.; Noll, T. G.: "ASIP-eFPGA architecture for multioperable GNSS receivers", Proc. of SAMOS Workshop, 2008, Samos
- Kappen, G.; Pieper, V.; Kurz, L.; Noll, T. G.: "Implementation and Analysis of an SDR Processor for GNSS Software Correlators", Proc. ION, 2008, Savannah, Georgia, USA



**Thank you very much
for your kind attention !**

