

Optimization Algorithms for Dynamic Reconfigurable Embedded Systems

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Reconfigurable hardware components such as FPGAs is used more and more in embedded systems, since such components offer a sufficient capacity for a complete SoC(System on a Chip) or even NoC(Network on a Chip). In order to use efficiently the dynamic reconfiguration possibility on such components, one needs a support in the form of operating systems to manage both software and reconfigurable hardware processes. For this support, suitable reconfigurable hardware model, and optimization methods are required. Our goal is the investigations of optimal strategies, methods, and architectures for controlling and use of the newest and future generations of reconfigurable hardware.

We target a Dynamic Reconfigurable System(DRS) which is made up of a soft core such as CPU(Central Processing Unit), and a Reconfigurable Processing Unit(RPU). In modelling of hardware resources, the characteristics like non-interruption of hardware tasks, reconfiguration overhead, communication model are considered. Task and resource managements on the DRS are on-line problems, that we investigate the optimal solutions for them.

Run-time space allocation, also known as temporal placement or on-line placement is a central part in reconfigurable computing system. In the on-line placement problems, for placing a new module, first we should identify the set of potential sites to place the new task. In most of the work, maximal empty rectangles will be stored for identifying the possible regions. But this method has a high complexity and modules should be placed always in the bottom left corner of an empty rectangle. Considering the fact that the set of empty rectangles grows much faster than the set of placed rectangles (tasks) leads us to manage the occupied space rather than the free space on the device. We identify the impossible regions, by computing the potential overlapping of the new module with other placed modules. In the second step in on-line placement, the best position to place the new module according to a set of given criteria should be selected. In contrast to existing methods, instead of using heuristic approaches such as best-fit or first-fit, we optimize the communication cost of the new module with the placed modules and input/output ports of the device. We have suggested two algorithms for this optimization, one in terms of Euclidean distance in the communication cost, and an optimal one by Manhattan distance.

To determine how the communications should be realized, optimal routing algorithms are needed. For on-line routing, there are two scenarios: packet routing and circuit routing. We are now implementing a packet routing approach on Xilinx FPGA for communication of placed modules, but our concentration is to develop optimal circuit-switching routing methods, which is more technology independent.